A circuit diagram of the EHI imager is shown in Fig. 6.7.1. The EHI pixel is composed of two photodiodes. One works as the integrating-type photodiode (D2) for imaging, and the other works as the micro solar cell (D1) for energy harvesting. The pixel contains 4 NMOS transistors, M1 is for resetting the FN node, M2 and M3 are the source follower and select transistors. M4 is the enable transistor for energy harvesting. Anodes of D1s are connected to an energy-harvesting bus (EHB). Depending on the operation mode, EHB is either connected to ground (imaging mode, IM) or to an on-chip charge pump (CP) or directly to a load (energy harvesting mode-EHM). In IM, D1 and D2 work in parallel to discharge the FN node. The FN node voltage is buffered to a column analog signal processor (ASP) like a regular 3T APS pixel, and processed for imaging. During EHM, M4 is turned on shorting D2, and forcing D1 to work as a regular solar cell.

Timing diagrams for IM and EHM are shown in Fig. 6.7.2. A 1.2V supply makes buffering FN node voltages impossible because of the high threshold voltage of the NMOS transistor (+0.8V), and its backgate bias. Thus, pixel reset and select signals are both boosted while SBT is utilized for PSF by boosting the pixel supply voltage (V_{DD}) during row read. The pixel supply (V_{DD}) is driven by the supply bootstrapping circuit (Fig. 6.7.1). When IN is asserted high (V_{DD}), V_{DD} is boosted close to 2V_{DD} and drops to V_{DD} when IN is low. An on-chip 170pf booster capacitor is used to provide a very low PSF current consumption. Charge-based column ASPs, coupled to a single global charge amplifier [5], and a 10b SB-SAR ADC are used in the design to achieve low power. Reference currents are generated on chip. 8b programmable current DACs are used to generate bias currents with 60na steps at 1.2V supply.

The pixel layout is shown in Fig. 6.7.3. Die area for the imager is 2×2mm² while the pixel size is 21µm². An Nwell/P+P-sub structure is used to form D1 (P+/N-well) and D2 (N-well/P-sub) [4]. P+ is directly connected to EHB, while the N-well is connected to the drain of reset (M1) and gate of PSF (M2) transistors. A pixel fill factor of 32% was achieved due to the N-well design rules, the extra transistors of EHB and ground signals. Two operation modes are available during EHM: direct drive (DD) and charge pump (CP). In both cases, all D1s are connected between EHB and ground through M4. During CP-EHM, all control signals except CP clock are stopped. The reference generator and IDACs are also turned off right after the CP comparator bias is sampled. Thus, only the CP comparator consumes static power. External capacitors C_{P1}=1µF and C_{P2}=10nF are used to measure CP efficiency and rise time. The measured rise time is 270ps achieving an efficiency level between 70% and 89%, depending on the level. Rise time depends on the C_{P1} value and can be reduced further by choosing it close to C_{P2}. During CP-EHM, total power consumption of the chip is <1µW. CP control logic is designed such that the charge from C_{P2} is transferred to C_{P1} completely in 8 clock cycles while sequentially triggering clock phases as shown in Fig. 6.7.2.

Energy-harvesting efficiency and current-voltage/power-voltage (I-V/P-V) characteristics of the EHI pixels are measured for different light levels between 1,000lux (overcast daylight) and 60,000lux (sunny daylight) at DD-EHM by using an external load resistor (R_{L}), as shown on Fig. 6.7.4a. At the maximum power point (MPP), the 54×50 EHI pixel array produces 380mV and 8.75µA, resulting in 3.35µW of power for 60,000lux illumination. Power reduces to 2.1µW and 1.0µW for 20,000lux and 1,000lux (normal and overcast daylight), respectively. Short-circuit voltages of the cells are between 400 and 450mV. Harvesting efficiency is also measured to be around 9% as shown on Fig. 6.7.4b at the MPP of the EHI pixels.

Imaging mode measurements are performed at various supply voltages (1.2 to 1.6V), 1.4fps frame rate, 4x pixel saturation, and optimum bias settings with which the EHI imager produces low FPN images, as shown on Fig. 6.7.5. Full chip power at 1.5V is 27.4µW. Detailed block powers are measured at 1.2V. Pixel array power consumption is directly measured to be 22nW resulting in 26.4nW power consumption. This is achieved by using SBT while biasing each PSF to 78nA, and fast row sampling resulting in 0.52% per frame PSF activity. The SB-SAR ADC consumes 3.13µW while running at 20kHz, less than half of its maximum speed. The global amplifier consumes 2.17µW, while IDAC and reference generator consume 3.21µW. 16 timing and control signals are generated off chip. Thus, the largest power is consumed on pads, which is about 5.64µW. Total leakage current when the chip is powered down is 80nA. As a result, total power consumption is 14.25µW for 1.2V supply and 7.4fps.

An imager figure of merit (iFOM) is defined to quantify the total energy consumption per pixel for one code quantization of effective pixel signals and for driving them off chip. Thus, total power consumption of the chip is used for calculating iFOM in J/pixel-code. Both FOM (from [6]) and iFOM are calculated and shown on Fig. 6.7.6. The EHI imager has 1.32pW/frame-pixel FOM and 696µJ/pixel-code iFOM achieving lowest power consumption. This does not include the EHI imager’s ability to harvest energy from light and could be further reduced if a low-power MPP tracer and regulator is incorporated on-chip to drive chip power from a larger CP_{1}.

Acknowledgments:
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References:
Figure 6.7.1: Circuit diagram of the EHI CMOS APS imager.

Figure 6.7.2: Timing diagram of the EHI CMOS APS imager.

Figure 6.7.3: Energy harvesting and imaging (EHI) pixel layout.

Figure 6.7.4: Measured energy-harvesting characteristics of the EHI imager: (a) voltage-current/voltage-power (I-V/V-P) curves, (b) input-output power characteristics at maximum power point (MPP) for harvesting efficiency.

Figure 6.7.5: Full chip power consumption and captured images at different supply voltages.

Figure 6.7.6: Performance comparison of the EHI imager and similar low-power imagers from [5] and [6].
Figure 6.7.7: Micrograph of the EHI imager chip.