An On-chip Ramp Generator for Single-Slope Look Ahead Ramp (SSLAR) ADC

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Abstract—An on-chip ramp generator was developed for single-slope look-ahead ramp (SSLAR) analog-to-digital converter (ADC) integrated in a column-parallel CMOS image sensor. Ramp generator is the central part of a new ADC algorithm which uses modified single-slope ramp (SSR) ADC timing. Ramp block designed such a way that it allows wide output voltage ranges as well as code hopping, code fall back and look-ahead operations in column-parallel ramp ADC. Ramp generator was fabricated using 0.5μm, 2P3M CMOS technology. Ramp generator composed of 10-bit synchronous counter, switched-capacitor based voltage steering circuits, output buffer and logic circuits. Effective layout area of ramp generator is 0.3mm².

Keywords: CMOS image sensors; CMOS APS; column parallel ADC; single-slope ramp ADC; single-slope look-ahead ramp ADC; ramp generator.

I. INTRODUCTION

Column-level analog-to-digital converters (ADC) in CMOS image sensors are used for high speed read out of large pixel arrays with low system level power consumption [1, 2]. Successive approximation register (SAR), single or multiple slope ramp (SSR/MSR), and algorithmic ADC topologies are the three most widely used topologies in CMOS APS imagers. SAR-ADC provides best speed performance. Main issue is the limitation of ADC resolution without introducing much image artifact in the form of fixed pattern noise (FPN). Higher resolution also results in larger layout size, and requires better processing and component characteristics. Single slope ADC, on the other hand can provide higher ADC resolution with the cost of the conversion time, and smaller silicon footprint. Speed issue is typically addressed by introducing multiple ramp operation with the cost of silicon area. Algorithmic ADCs provides relatively good ADC resolution, yet, it suffers from design and integration difficulties, an associated larger size and noises. Among these topologies, SSR-ADC provides good balance between noise, size and resolution, if the speed issue is addressed, [3]. A new single-slope ramp ADC topology called single-slope look-ahead ramp (SSLAR) ADC was reported for column parallel CMOS APS imagers to overcome the speed issue in SSR ADC, [4]. In this paper, central part of this new ADC topology which is a unique ramp generator and counter is reported.

This paper comprises of following sections. The new SSLAR ADC topology is reported in Section II. Underlying new algorithm which leads to the design of jump and fold back ramp generator topology is also explain in this section. General overview of on-chip ramp generators and proposed new ramp generator architecture were explained in Section III. Layout and other design issues are also discussed in this section. Section IV describes the measurement results. Finally, section V gives the conclusion.

II. SINGLE-SLOPE LOOK-AHEAD RAMP (SSLAR) ADC

Single-slope ramp ADC (SSR-ADC) is very suitable for column-parallel integration in CMOS image sensors because of its simple structures (Fig. 1). In column parallel CMOS imagers, m-number of ADCs are integrated along with column sample and hold (CSH) circuits. Each ADC on the column receives global ramp voltage and n-bit digital counter signals. The SSR-ADC on each column is composed of a comparator and n-bit transparent latches. One of the comparator input is driven by a global ramp signal, while the other is driven by the CSH. Comparator output changes state when the ramp signal becomes larger than the CSH signal. It provides a clock signal to the transparent latches enabling transparent latch to hold the last global counter bits. Thus, proper operation requires counter and ramp signals to be synchronized. SSR-ADC operates at a much slower speed (2° clock) than that of SAR-ADC (n clock), and requires much less power and a smaller silicon area. Speed issue of SSR ADC in CMOS image sensors is addressed by a new ADC algorithm and topology called single-slope look-ahead ramp ADC (SSLAR-ADC) [4]. Integration of new SSLAR ADC in column-parallel CMOS imagers is shown in Fig. 2. Two new blocks are introduced in the new architecture.

![Figure 1. Column-parallel integration of SSLAR ADC in CMOS imagers.](image-url)
They are the look-ahead controller (LAC) and column predictors. In SSLAR ADC, ramp generator and the counter was modified to accommodate look, jump, and fall back operations. Detailed operation timing of LAC, counter, and ramp generator in proposed architecture are shown in Fig. 3. Ramp generator and counter receive two digital control signals from the LAC block: look and jump. When look signal is activated ramp output jumps ahead k-steps while counter jump ahead k/2-bits. If jump signal is logic-1 while look signal going from logic-1 to logic-0, then the ramp output continues from jumped analog level. In this case, counter jumps k/2-bits more to count from k-bits ahead from the pre-jump count value as seen in Fig. 3a. If jump signal is logic-0 while look signal going from logic-1 to logic-0, then the ramp falls back k-steps to the original level. In this case, counter also falls back k/2 bits to pre-jump level as seen in Fig. 3b. For every guaranteed jump operation, (k-h) clock cycle is saved resulting in increased conversion speed. For every denied jump, h clock cycle is lost.

This conversion algorithm was designed for column parallel SSR ADC, and it was shown that it would provide speed-up for real life image capturing in CMOS image sensors. [4].

III. ON-CHIP RAMP GENERATOR DESIGN

A. Ramp Generator Topologies

In SSLAR-ADC architecture, it is important to have an on-chip ramp generator to accommodate novel functions to reduce conversion time of ADC. There are different kinds of on-chip ramp generator topologies available as shown in Fig. 4.

Ramp generator topologies can be categorized depending on the nature of ramp signal at the output as shown in Fig. 4. Generated ramp signals are continuous in time and either continuous or discrete on output levels. Continuous (analog) ramp generators produce continuous, smooth ramp signal without any distraction while ramping [5,6]. They are controlled through either by current or by voltage. The main advantage of this type is that it requires small area. However, ramp rate is difficult to control in different operating conditions. Ramp rate can be controlled digitally to correct these environment variations. Discrete (digital) ramp generators produce discrete ramp signal or ramping with small steps at regular intervals of time, [7]. Averaging the discrete ramp signal gives the continuous ramp signal. Most of the discrete topologies are derived from digital to analog converter (DAC) topologies. Flexibility in controlling or manipulating ramp signal is done by using the key digital control blocks such as counters and shift registers. Using these blocks, it is easy to control the ramp signal. One drawback is the larger silicon area is required compared with the continuous ramp generators.

B. Proposed Ramp Generator Topology for SSLAR

Working of proposed ramp generator is illustrated with conceptual 10-bit version of a digital to analog converter shown in Fig. 5. It consists of an analog buffer, an array of binary weighted capacitors, and switches (S₀₋₉, S₀₋₉, S₀₋₉) which connects the capacitor plates to certain voltage. The switches (S₀₋₉) are controlled by the 10-bit digital input corresponding to least significant bit (LSB) to most significant bit (MSB). Depending on the switch condition, the bottom plate of capacitor is either connected to Vᵱᵣᵱ or Vᵱᵣₑ voltage level.

In the first, switch S₀₋₉ is closed and set the top plates of the binary capacitances and the Vᵱᵣₑ to Vᵱᵣₑ. When digital input equals to ‘0’, the bottom plate of the capacitors are connected to Vᵱᵣₑ so that the top and bottom plate of the capacitor are at same potential and net charge on any capacitor will be zero. When 10-bit digital inputs are incremented, there will be a charge distribution between the two sets of capacitors. Cₒ₋₉ and Cₒ₋₉ is the total capacitance between node Vₒ₋₉ and Vₒ₋₉ node. Similarly Cₒ₋₉ is the equivalent capacitance between node Vₒ₋₉ and Vₒ₋₉. This charge distribution results a
voltage change on output node as given by equation (1).

\[
V_{out} = \left( \frac{V_{top} - V_{ref}}{C_{top}} + V_{ref} \right) \cdot C_{top} + V_{ref} \tag{1}
\]

Voltage on node \( V_{out} \) can be increased in discrete step sizes \( (V_{step}) \) if the digital inputs are increased by 1-LSB at regular time intervals. In order to control the switches or to generate n-bit digital input at regular intervals, n-bit synchronous counter can be used. The reason of using the synchronous counter is that whenever capacitors are switching between \( V_{a} \) and \( V_{top} \) involves charge pumping to or from the node \( V_{out} \). Especially when the digital inputs change from \( 0<11111111111 > \) to \( 0<10000000000 > \), it involves switching or pumping charge on \( \frac{V_{top} - V_{ref}}{C_{top}} \) and dumping charge from the other capacitors to \( V_{a} \). If switching does not take place simultaneously, output node results in a big glitch on the output voltage during the counter increment.

The above explained 10-bit DAC topology is modified to attain 10-bit ramp signal with look and jump features for SSLAR ADC. There are different ways to achieve the required function. In order to jump and fall back as quick as possible, an additional capacitor \( C_{jump} \) is included. The value of \( C_{jump} \) depends on jump voltage range at the \( V_{out} \) during ramping operation from \( V_{a} \) to \( V_{top} \). An additionally combinational logical circuit is added to 10-bit synchronous counter. Fig. 6 shows the additional changes made to 10-bit synchronous counter. There are two signals received from SSLAR ADC to control look and jump function in 10-bit ramp block. Depends on the jump control input, the combination logic introduced in 10-bit counter adds binary weighted numbers to the present value of the 10-bit counter value. For example, when jump equals to 0, it does not affect the normal operation of the counter. When jump asserted to 1, the combinational logic at the output 4th bit adds 16 to the previous state value. As long as jump is asserted '1', counter is incremented by 16 during each positive edge of the clock. When hold equals to '0', counter holds four LSB bits and holding or jumping 16 LSB depends on jump signal.

The 10-bit look ahead ramp generator is shown in the Fig. 7 with incorporated logic and signals. The positive edge D-flip flop synchronizes look ahead jump or fall back transitions of ramp generator with clock. The synchronized look signal controls the switch \( S_{ jmp \_top} \) to pump or dump charge from the node \( V_{out} \) through \( C_{jump} \). The Switch \( S_{jump} \), is controlled during negative edge of the master clk. When look signal is activated or logic-0, the synchronized look signal swaps the switch \( S_{ jump} \) to pump charge from \( V_{a} \) to \( V_{out} \) and simultaneously holds the 10-bit counter. Introduced charge pulls up the node \( V_{out} \) to k-step ahead. During activation of the look signal, if the jump signal changes from logic-1 to 0, the counter incremented by 16-LSB. Upon deactivation of look signal, the \( C_{jump} \) is removed and the k-steps introduced by \( C_{jump} \) is compensated by 16-LSB increment in counter or capacitor bank. Until next activation of the look signal, ramp generator ramps with discrete steps. While look signal is activated and jump signal is not changes or logic-0, upon deactivation of look signal switches \( S_{ jmp \_top} \) to dump introduced charge or k-step to GND. And ramp signal falls backs k-steps and continuous with discrete steps. Detailed timing diagram of the new look ahead jump ramp generator for SSLAR ADC is shown in Fig.8. The value of \( C_{jump} \) is chosen such that to compensate the 16-LSB increment in counter or capacitor bank.

C. Layout Design

The proposed design is fabricated in a 0.5μm PMCMOS process. Layout of 10-bit on-chip look ahead ramp generator is shown in Fig.10. Effective area of the on-chip ramp generator block is 0.33μm². The unit capacitance, \( C_{cells} \) selected was 16fF and \( C_{jump} \) of 143fF.

IV. Measurement Results

Functional verification such as jump, fall back, single step and the intrinsic linearity characteristics such as differential and integral non-linearity (INL/DNL) are tested for fabricated 10-bit look ahead ramp generator. There are different approaches available to test ramp blocks using off chip components. One of the common methods is to use external high resolution ADC. On-chip LJRAG's 10-bit analog output was sent to with this 12-bit off-chip ADC. One main problem with this testing setup shown in Fig.9 is filtering error data from external noise.
Fig. 11 shows continuous look ahead jumps followed by regular discrete steps. From 12-bit ADC data, when the jump is activated, ramp looks ahead with a precision of 31±1 LSB, and fold back 16-LSB. In proposed design, 31-LSB jump is not compensated by 16 LSB jump in counter, that is why ramp falls back 16-LSB back even jump is activated. If the jump is not received during activation of lock signal, the ramp fold backs to original analog voltage level with ±1LSB precision shown clearly in Fig. 12. Those ±1LSB errors are caused by external noise.

The proposed 10-bit LJR in have DNL of +6 to -8 LSB. But, by ignoing DNL of every 6ths bit change (64 LSB’s), and critical switching DNL especially from <0111111111> to <1000000000>, the resultant DNL is ±2 LSB. Poor switching, charge injection and leakage current, external noise degraded the operation of the proposed design during critical switching conditions. This leads 10-bit LJR not to reach the full scale range and affects the INL of the DAC around 60LSB.

V. CONCLUSION AND FUTURE WORK

The proposed design presented in this paper demonstrates the use binary weighted DAC with novel feature for SSLAR-ADC. Measurement results show that look ahead ramp generator topology results good performance in achieving look ahead jump and fold back in ramp signal. On the other hand, design issue like capacitor switching, charge injection and leakage current results in bad intrinsic characteristics of the DAC. The future work relies on improving and implementing the same function in different topologies with programmable k-step look ahead jump for better intrinsic characteristics with high precision.

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VII. REFERENCES


