A Single-Slope Look-Ahead Ramp (SSLAR) ADC for Column Parallel CMOS Image Sensors

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Abstract—A new analog-to-digital converter (ADC) algorithm was proposed for column-parallel CMOS image sensors. The proposed algorithm uses single-slope ramp ADC timing on a column-parallel CMOS image sensor. Single-slope look-ahead ramp (SSLAR) ADC algorithm introduces code hopping, fall back, and look-ahead operations considering statistical distribution of the sampled row of information on column samples and hold circuits. The algorithm was run on an array of standard images for performance comparison. It was also run on 300 random images to get speed and jump step trends. It was determined that the algorithm results in increased ADC speed; improving frame rate of the CMOS image sensor without degrading image quality. The new ADC provides 1.7x to 3.5x ADC speed improvement with less than 1.0x image quality degradation which a normal human eye cannot detect. Algorithm trades ADC speed and power consumption with image quality. The proposed algorithm shortens ADC conversion time resulting in reduced power consumption and increased frame rate of the column-parallel CMOS image sensor.

Keywords—CMOS image sensors, CMOS APS, column-parallel ADC, single-slope ADC, look-ahead ADC, ADC algorithm.

I. INTRODUCTION

Several different types of column parallel ADCs have been used in CMOS image sensors. Successive approximation register (SAR) type ADC is one of them. SAR-ADC provides a small silicon footprint, high conversion rate, and consumes very little power [1, 2]. It converts analog input with a very low latency. However, one limitation that SAR-ADCs face in CMOS image sensor applications is the resolution, which is limited by the capacitance mismatch. Thus, for high resolution CMOS image sensors a second type of column parallel ADCs the single (or dual) slope ramp (SSR) ADC are preferred [3]. Nonetheless, higher resolution comes with the price of latency and limits their use in high-speed applications. To address this speed issue, a new type of SSR-ADC was introduced [4]. This ADC uses multiple ramp signals to overcome the speed issue. However, this architecture requires a complicated on-chip ramp generator degrading the power advantage of column parallel architecture used in CMOS image sensors.

In this work, we introduce a new ADC algorithm and column parallel ADC architecture integrated on a column-parallel CMOS image sensor to reduce SSR-ADC's latency without degrading the image quality and integrity. The new ADC introduces code hopping, fall back, and code look-ahead operations considering statistical distribution on the sampled row signals. We call this architecture a single slope look-ahead (SSLAR) ADC architecture. This paper focuses on introduction of the SSLAR ADC algorithm and its implementation and simulation using MATLAB to verify the proper operations. The SSLAR algorithm and the architecture are introduced in section II. Section III describes the simulation results of the algorithm. Section IV is dedicated to discussion and future work.

II. SINGLE-SLOPE LOOK-AHEAD RAMP ADC

A. Single-Slope Ramp ADC

Single-slope ramp ADCs (SSR-ADCs) are one of the simplest ADC architectures used in ICs for converting analog signals into digital bits [5]. SSR-ADC is very suitable for column-parallel integration in CMOS image sensors as shown in Fig. 1. In column parallel architectures, m-number of ADCs are integrated together following column sample and hold (CSH) circuits of column parallel CMOS image sensors. They work in parallel to convert m-number of analog signals at the same time. Each ADC on the column receives global analog ramp and n-bit digital counter signals. The SSR-ADC is composed of a comparator and n-bit of transparent digital latches. The comparator is driven by the global ramp, and provides a clock signal to the transparent latches. The comparator output changes state when the ramp signal becomes larger than the CSH signal driving the comparator’s other input. When the comparator changes state, transparent latch hold the last global counter bits. For proper operation, counter and ramp signals have to be synchronized. 3-bit operation timing of SSR-ADC integrated on a CMOS imager column is shown in Fig. 2.

SSR-ADC operates at a much slower speed than that of SAR-ADC and it requires much less power and a smaller IC area. However, analog to digital conversion speed of SSR-ADC is slow and it requires 2^n times the master clock cycle (Cclk). For example, a 10-bit representation of an analog signal can be converted into digital form after 1024 clock cycles. Compared with other ADC topologies such as flash ADC (require only 1 clock cycle for conversion) or successive approximation (SAR) ADC (require n-clock cycles for conversion), SSR-ADC is the slowest.
LAC achieves these tasks providing timing signals to the modified counter and ramp generators. It also has two analog reference inputs, \( V_{ref1} \) and \( V_{ref2} \). \( V_{ref1} \) is larger than \( V_{ref2} \). \( V_{ref2} \) is used for charging the analog prediction bus. Depending on the amount of charge that is injected by column predictors, column prediction bus voltage surpasses \( V_{ref2} \) level, triggering code jump operations in ramp generator and counters. Code jump operation is triggered when the effective jump signal becomes positive which is given by the following equation:

\[
\Delta V_{\text{jump}} = V_{\text{pred}} - V_{\text{ref2}} = \frac{k \cdot V_{\text{supply}}}{m} - V_{\text{ref2}} > 0
\]  

In this equation, \( m \) is the number of columns on imager column, \( k \) is the number of columns that switch from logic-0 to logic-1 for a given ramp voltage, and \( V_{\text{supply}} \) is the supply voltage of the ADC.

The timing of typical ramp generator and counter used in SSR ADC has to be modified for SSLAR-ADC topology. Detailed operation timing of LAC, counter, and ramp generator in proposed architecture are depicted in Fig. 4. The ramp generator gets two digital control signals from the LAC block: look and jump. When look signal is activated, ramp output \( V_{\text{ramp}} \) jumps \( k \)-steps ahead while counter jumps \( (k/2) \)-bits ahead. If jump signal is logic-1 while look signal going from logic-1 to logic-0, then the ramp output continues from jumped analog ramp level. In this case, counter jumps \( (k/2) \) bits to count from \( k \)-bits ahead from the pre-jump count value \( t \) as seen in Fig. 4. If the jump signal is logic-0 while the look signal going from logic-1 to logic-0, then the ramp output falls back \( k \)-steps to the original level before the look operation. In this case, the counter also jumps \( (k/2) \) bits back to count from the pre-jump count value \( t \).

In the best case, where all column voltage values are in one \( k \)-step range of the ADC input, conversion time of the SSLAR ADC is given by the following equation. Uniform input distribution is the worst case for SSLAR ADC conversion time. Equation (2) defines the best and worst case conversion times for the SSLAR ADC. For arbitrary input voltages, SSLAR ADC conversion time can be defined with the best case with a proportional constant \( (a) \) which is less than unity.

\[
(2^n - h) \times T_{\text{clk}} \geq T_{\text{SSLAR}} \geq \left( \frac{2^n}{k} \right) \cdot (k - h) + h \times T_{\text{clk}}
\]  

In the best case, where all column voltage values are in one \( k \)-step range of the ADC input, conversion time of the SSLAR ADC is given by the following equation.
Comparing the best case scenario of SSLAR ADC with the SSR-ADC conversion time, speed-up ratio for the SSLAR-ADC can be found with the following equation.

$$S_{\text{speed-up}} = \frac{T_{\text{SSLAR}}} {T_{\text{SSLAR,cout}}} = \frac{2^n} {\alpha \cdot \left( \frac{2^n}{k} \cdot (k \cdot h) + h \right)}$$  (3)

The average speed up characteristics of the new ADC can be determined by running the algorithm on a large number of image databases. It will be reported in the next section.

Speed can be translated into two parameters of the image sensor. One is the image quality that the ramp jump operation results in while increasing the speed. The other one is the power consumption of the ADCs. Since ADC conversion time is reduced, active power consumption is reduced at the same rate as the speedup. Thus, the higher the speedup achieved, the lower the power consumption. The higher the speed up on the other hand, the larger the number of jumps and as a result, the poorer the image quality. These trade-offs are explored and quantified in the following section.

III. SIMULATION OF SSLAR-ADC ALGORITHM

A. SSLAR-ADC Algorithm

SSLAR-ADC algorithm requires 3 critical parameters to be set during operation. They are the jump step size (k) in number of bits, LAC threshold (s) in terms of number of column comparators changing states (cni) during look-ahead. Jump step size is used by both the ramp generator and the ramp counter during the look-ahead operation. The SSLAR-ADC algorithm steps are shown in Table I.

B. MATLAB Simulation of SSLAR-ADC Algorithm

The SSLAR-ADC algorithm listed in Table I was implemented in MATLAB. A standard gray image of 256x256 image of "LENA" was used. The image has 256 quantization levels or 8-bit resolution. The jump steps (k) between 1 and 16-LSB and threshold levels (s) of 2, 4, 6, 8, 10, 12, 14, and 16-LSB was considered during simulation to plot both speed up and Mean-square error (MSE) rated in percent of full scale. MSE is a typical picture quality measure that is used for evaluating picture processing. [6]. MSE in percent of ADC full scale is given with the following equation.

$$MSE = 100 \frac{\sum_{x=1}^{X} \sum_{y=1}^{Y} \left| P_{\text{org}}[x,y] - P_{\text{SSLAR}}[x,y] \right|^2} {x \cdot y}$$  (4)

Fig. 5 shows the effect of SSLAR-ADC algorithm on image quality and conversion speeds for different jump steps and threshold levels. General trends of MSE and speed-up of the "LENA" picture assumed to be captured by a CMOS image sensor containing SSLAR-ADC on board are shown in Fig. 6 and Fig. 7, respectively. SSLAR ADC provides higher speed up for higher threshold levels for jump steps between 3 to 8 LSBs. However, under such conditions image quality degrades which can be observed on Fig. 5.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>SSLAR-ADC ALGORITHM</th>
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<tbody>
<tr>
<td>Step 1:</td>
<td>Sample a row of pixels on CSH circuits,</td>
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<tr>
<td>Step 2:</td>
<td>Reset ramp generator and ramp counter.</td>
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<tr>
<td>Step 3:</td>
<td>Start ramp and counter.</td>
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<tr>
<td>Step 4:</td>
<td>Look ahead -LSB equivalent ramp analog output, and (k2)-LSB counter outputs</td>
</tr>
<tr>
<td>Step 5:</td>
<td>Check column predictors.</td>
</tr>
<tr>
<td>Step 6:</td>
<td>Is there enough column comparator change state in k-LSB range? IF YES: fall back k-LSB on ramp voltage and (k2)-LSB on counter output, ramp and count one LSB at a time for k-LSB, then go to Step 7. IF NO: Do not change analog ramp voltage, increment counter (k2)-LSB step, go to Step 7</td>
</tr>
<tr>
<td>Step 7:</td>
<td>Have we reached 2^n bit range? NO (go to Step 4), YES (go to Step 8)</td>
</tr>
<tr>
<td>Step 8:</td>
<td>Go to Step 1</td>
</tr>
</tbody>
</table>

Figure 5. Sample images show that threshold change affects image quality as well as conversion speed.

Figure 6. MSE versus jump steps for "LENA".
C. SSLAR-ADC Algorithm Trade-offs

Trends of the SSLAR ADC algorithm on image quality and ADC speed up were investigated by running 400 randomly selected black and white images [7]. Average MSE and speed up of these images were plotted for jump steps between 2 and 64, as shown in Fig. 8. Similar trends were observed from these 400 images as the “LENA” picture that with a proper selection of jump steps and the thresholds, more than four times (4x) speed increase is possible with less than 0.5% image quality degradation which cannot be detected by the normal human vision system. SSLAR ADC algorithm trades image quality with the ADC speed. Optimum step size and threshold can be observed from Fig. 8 for good image quality and high speed operations.

IV. CONCLUSION

A new ADC algorithm and architecture was proposed for column parallel CMOS image sensors. New ADC is based on single slope ramp (SSR) ADC architecture and introduces a new timing operation allowing image acquisition speed up without degrading the image quality. We call this new ADC architecture single slope look-ahead ramp (SSLAR) ADC due to the fact that new algorithm and added circuitry help predict number of pixels sampled on CSH on a certain ADC code range, and allows code range to be skipped or scanned. This code look-ahead capability allows faster ADC operation comparing the SSR ADC timing on column parallel CMOS architectures. While SSLAR ADC algorithm provides speed up, it introduces code errors of less than half of the jump step size in LSB. This results in degradation of image quality. For human eye not to observe these artifacts, image quality has to be maintained.

SSLAR ADC algorithm was simulated by using a single standard image (“LENA”) and 490 different gray scale images with 8-bit resolution. It was observed that for SSLAR ADC jump steps between 3 and 16 LSB and threshold between 6 and 12 LSB results in less than 1% image quality degradation and 1.7x to 3.5x ADC speed up can be achieved. Yet, image quality is traded with the ADC speed, SSLAR ADC architecture can work as SSR ADC when the jump step size and threshold of 1 LSB was chosen providing zero image quality degradation. This can be done by updating these parameters in one clock cycle allowing seamless mode switching.

V. REFERENCES