Chapter 8
Analog I/O
November 7, 2007

Analog to Digital Conversion

Basic Building Blocks

R2R Ladder Network

R/2R ladder networks provide a simple means to convert digital information to an analog output. Although simple in design and function, applying an R/2R resistor network to a real application requires attention to how the device is specified. Output errors due to resistor tolerances are often overlooked in the design of the digital to analog conversion (DAC) circuit and in the selection of the R/2R ladder itself. This application note identifies these issues, provides methods for calculating R/2R resolution and accuracy and a means to better specify R/2R ladder networks.

Resistor ladder networks provide a simple, inexpensive way to perform digital to analog conversion (DAC). The most popular networks are the binary weighted ladder and the R/2R ladder. Both devices will convert digital voltage information to analog, but the R/2R ladder has become the most popular due to the network’s inherent accuracy superiority and ease of manufacture. Figure 1 is a diagram of the basic R/2R ladder network with N bits. The “ladder” portrayal comes from the ladder-like topology of the network. Note that the network consists of only two resistor values; R and 2R (twice the value of R) no matter how many bits make up the ladder. The particular value of R is not critical to the function of the R/2R ladder.

The binary weighted ladder shown in Figure 2 requires double multiples of R as the number of bits increase. As the ratios of the resistors become more and more obtuse in a binary weighted network, the ability to trim the resistors to accurate ratio tolerances becomes

Figure 1. N bit R2R resister ladder network

diminished. More accurate ratios can be obtained in a resistor network with consistent, similar values as in the R/2R network. The R/2R network provides the most accurate method of digital to analog conversion.

**Figure 2. Binary weighted resistor ladder network**

Let’s take a look at how an R/2R ladder works. The expression “Term.” In Figure 3 is the termination resistor and is connected to ground. The termination resistor assures that the Thevenin resistance of the network as measured to ground looking toward the LSB (with all bits grounded) is R as shown in Figure 3. The Thevenin resistance of an R/2R ladder is always R — regardless of the number of bits in the ladder.

**Figure 3. Thevenin Resistance**

Digital information is presented to the ladder as individual bits of a digital word switched between a reference voltage (Vr) and ground (Figure 4). Depending on the number and location of the bits switched to Vr or ground, Vout will vary between 0 volts and Vr. If all inputs are connected to ground, 0 volts is produced at the output, if all inputs are connected to Vr, the output voltage approaches Vr, and if some inputs are connected to ground and some to Vr then an output voltage between 0 volts and Vr occurs. These inputs (also called bits in the digital lingo) range from the Most Significant Bit to the Least Significant Bit.

As the names indicate, the MSB, when activated, causes the greatest change in the output voltage and the LSB, when activated, will cause the smallest change in the output voltage. If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is: Vout = Vr/2N where N is the bit number. For bit 1, Vout = Vr/2, for bit 2, Vout = Vr/4 etc. The table shows the effect of individual bit locations to the Nth bit. Notice that since bit 1 has the greatest effect on the output voltage it is designated the Most Significant Bit.

Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to
calculate \( V_{\text{out}} \). The expected output voltage is calculated by summing the effect of all bits connected to \( V_r \). For example, if bits 1 and 3 are connected to \( V_r \) with all other inputs grounded, the output voltage is calculated by: \( V_{\text{out}} = \frac{V_r}{2} + \frac{V_r}{8} \) which reduces to \( V_{\text{out}} = \frac{5V_r}{8} \).

![Figure 4. Switched R2R resistor ladder network](image)

The \( R/2R \) ladder is a binary circuit. The effect of each successive bit approaching the LSB is \( 1/2 \) of the previous bit. If this sequence is extended to a ladder of infinite bits, the effect of the LSB on \( V_{\text{out}} \) approaches 0. Conversely, the full-scale output of the network (with all bits connected to \( V_r \)) approaches \( V_r \) as shown in equation (1).

\[
\lim_{N \to -\infty} \sum_{i=1}^{N} \frac{1}{2^i} = V_r \quad (1)
\]

The full-scale output is less than \( V_r \) for all practical \( R/2R \) ladders, and for low pin count devices the full-scale output voltage can be significantly below the value of \( V_r \). Equation (2) can be used to calculate the full-scale output of an \( R/2R \) ladder of \( N \) bits.

\[
\text{Full Scale Output Voltage} = \left( V_r \right) \sum_{i=1}^{N} \frac{1}{2^i} \quad (2)
\]

An \( R/2R \) ladder of 4 bits would have a full-scale output voltage of \( 1/2 + 1/4 + 1/8 + 1/16 = 15V_r/16 \) or 0.9375 volts (if \( V_r=1 \) volt) while a 10 bit \( R/2R \) ladder would have a full-scale output voltage of 0.99902 (if \( V_r=1 \) volt).

**Resolution and Accuracy**

The number of inputs or bits determines the resolution of an \( R/2R \) ladder. Since there are two possible states at each input, ground or \( V_r \), (also designated as “0” or “1” in digital lingo for positive logic) there are \( 2^N \) combinations of \( V_r \) and ground to the inputs of an \( R/2R \) ladder. The resolution of the ladder is the smallest possible output change for any input change to the ladder.
and is given by $1/2N$ where $N$ is the number of bits. This is the output change that would occur for a change in the least significant bit. For a 10bit R/2R there are $2N$ or 1024 possible binary combinations at the inputs. The resolution of the network is $1/1024$ or 0.0009766. A change in state at the LSB input should change the output of the ladder by 0.09766\% of the full scale output voltage.

The output accuracy of the R/2R ladder is typically specified in terms of full-scale output $\pm$ some number of least significant bits. R/2R ladders are usually specified with output accuracies of $\pm 1$ LSB or $\pm 1/2$ LSB. For example, a $\pm 1/2$ LSB specification on a 10 bit ladder is exactly the same as $\pm 0.04883\%$ full-scale accuracy.

The ladder function is not affected by the value of R (within normal resistance ranges). This would indicate that the absolute tolerances of the resistors making up the ladder are of minimal importance. Then what controls the accuracy of the ladder output? The ladder operates as an array of voltage dividers whose output accuracies are solely dependent on how well each resistor is matched to the others. Ideally, resistors within the ladder are matched so that the voltage ratio for a given bit is exactly half of that for the preceding bit.

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Operational Amplifiers

Operational Amplifiers (OAs) are highly stable, high gain dc difference amplifiers. Since there is no capacitive coupling between their various amplifying stages, they can handle signals from zero frequency (dc signals) up to a few hundred kHz. Their name is derived by the fact that they are used for performing mathematical operations on their input signal(s). Figure 5 shows the symbol for an OA. There are two inputs, the inverting input (-) and the non-inverting input (+). These symbols have nothing to do with the polarity of the applied input signals.

![Figure 5. Symbol of the operational amplifier. Connections to power supplies are also shown.](http://www.chem.uoa.gr/applets/AppletOpAmps/Text_OpAmps2.htm)
The output signal (voltage), \( V_o \), is given by: 
\[ V_o = A(V_+ - V_-) \]

\( V_+ \) and \( V_- \) are the signals applied to the non-inverting and to the inverting input, respectively. \( A \) represents the open loop gain of the OA. \( A \) is infinite for the ideal amplifier, whereas for the various types of real OAs, it is usually within the range of \( 10^4 \) to \( 10^6 \).

OAs require two power supplies to operate, supplying a positive voltage (+V) and a negative voltage (-V) with respect to circuit common. This bipolar power supply allows OAs to generate output signals (results) of either polarity. The output signal (\( V_o \)) range is not unlimited. The voltages of the power supplies determine its actual range. Thus, a typical OA fed with -15 and +15 V, may yield a \( V_o \) within the (approximately) -13 to +13 V range, called operational range. Any result expected to be outside this range is clipped to the respective limit, and OA is in a saturation stage.

The connections to the power supplies and to the circuit common symbols, shown in Figure 1, hereafter will be implied, and they will be not shown in the rest of the circuits for simplicity.

Because of their very high open loop gain, OAs are almost exclusively used with some additional circuitry (mostly with resistors and capacitors), required to ensure a negative feedback loop. Through this loop a tiny fraction of the output signal is fed back to the inverting input. The negative feedback stabilizes the output within the operational range and provides a much smaller but precisely controlled gain, the so-called closed loop gain.

Circuits of OAs have been used in the past as analog computers, and they are still in use for mathematical operations and modification of the input signals in real time. A large variety of OAs is commercially available in the form of low cost integrated circuits. There is a plethora of circuits with OAs performing various mathematical operations. Each circuit is characterized by its own transfer function, i.e. the mathematical equation describing the output signal (\( V_o \)) as a function of the input signal (\( V_i \)) or signals (\( V_1, V_2, ..., V_n \)). Generally, transfer functions can be derived by applying Kirchhoff’s rules and the following two simplifying assumptions:

1. The output signal (\( V_o \)) acquires a value that (through the feedback circuits) practically equates the voltages applied to both inputs, i.e. \( V_+ \approx V_- \).

2. The input resistance of both OA inputs is extremely high (usually within the range \( 10^6 \) \(-\) \( 10^{12} \) MΩ, for the ideal OA this is infinite), thus no current flows into them.

**Inverting Amplifier**

The basic circuit of the inverting amplifier is shown in Figure 6. The transfer function is derived as follows: Considering the arbitrary current directions we have:

\[ i_1 = (V_i - V_+)/R_i \quad \text{and} \quad i_2 = (V_s - V_o)/R_f \]

The non-inverting input is connected directly to the circuit common (i.e. \( v_+ = 0 \) V), therefore (considering simplifying assumption #1) \( V_+ = V_s = 0 \) V, therefore:

\[ i_1 = V_i/R_i \quad \text{and} \quad i_2 = -V_o/R_f \]

Since there is no current flow to any input (simplifying assumption #2), it is

\[ i_1 = i_2 \]

Therefore, the transfer function of the inverting amplifier is

\[ V_o = -(R_f/R_i)V_i \]
Thus, the closed loop gain of the inverting amplifier is equal to the ratio of $R_f$ (feedback resistor) over $R_i$ (input resistor). This transfer function describes accurately the output signal as long as the closed loop gain is much smaller than the open loop gain $A$ of the OA used (e.g. it must not exceed 1000), and the expected values of $V_o$ are within the operational range of the OA.

\[ V_o = \frac{-V_{in}}{R_i} \cdot \frac{R_f}{R_i} \]

![Figure 6. Inverting operational amplifier circuit](image)

**Summing Amplifier**

The *summing amplifier* is a logical extension of the previously described circuit, with two or more inputs. Its circuit is shown in Figure 7. The transfer function of the summing amplifier (similarly derived) is:

\[ v_o = -(v_1/R_1 + v_2/R_2 + \ldots + v_n/R_n)R_f \]

Thus if all input resistors are equal, the output is a scaled sum of all inputs, whereas, if they are different, the output is a weighted linear sum of all inputs. The summing amplifier is used for combining several signals. The most common use of a summing amplifier with two inputs is the amplification of a signal combined with a subtraction of a constant amount from it (dc offset).

![Figure 7. Summing inverting amplifier](image)
Comparators

An integrated circuit "Voltage Comparator" is equivalent to an Operational Amplifier, such as the LM358 or LM324, with two NPN transistors added to the output of each amplifier. (Refer to the above schematic.) This arrangement produces an "Open Collector" output for each of the four comparators in an LM339 chip. Each output can sink 15 Milliamps and can withstand voltages of up to 50 Volts.

The output is switched ON or OFF depending on the relative voltages at the PLUS and MINUS inputs of the comparator, see the rules below. The inputs are quite sensitive and a difference of only a few millivolts between the two will cause the output to turn on or off. The LM339, LM393 and LM311 comparator chips can operate from a single or dual power supply of up to 32 volts maximum. When operated from Dual or Split power supplies the basic operation of comparator chips is unchanged except that for most devices the emitter of the output transistor is connected to the negative supply rail and not the circuit common. An exception to this is the LM311 which has a separate emitter terminal that can be connected to either. When operated from Dual or Split power supplies the input voltages can be above or below the common or zero voltage of the supply. If needed, one of the inputs can be connected to the common so that a 'Zero Crossing' detector is created.

The following drawing show the two simplest configurations for voltage comparators. The diagrams below the circuits give the output results in a graphical form. For these circuits the REFERENCE voltage is fixed at one-half of the supply voltage while the INPUT voltage is variable from zero to the supply voltage. In theory the REFERENCE and INPUT voltages can be anywhere between zero and the supply voltage but there are practical limitations on the actual range depending on the particular device used.

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3 Excerpts from http://home.cogeco.ca/~rpailey4/Comparators.html
**Input Offset Voltage and Hysteresis**

The effects of the input offset voltage can be countered by adding hysteresis to the circuit. This causes the reference voltage to change when the comparators output goes high or low. The effect is that as the input voltage slowly changes the reference voltage will quickly change in the opposite direction. This gives the comparator a "snap" action. See the following paragraphs for more information.

Hysteresis is the difference between the input signal levels at which a comparator turns off and turns on. A small amount of hysteresis can be useful in a comparator circuit because it reduces the circuit's sensitivity to noise, and helps reduce multiple transitions at the output when changing state. Sometimes, in a discrete design, there is a need to add an external resistor between the comparator's output and the positive input, creating a weak positive feedback loop. When the output makes a transition, the positive feedback slightly changes the positive input so as to reinforce the output change.

A mechanical analog of this effect can be found in many electrical switches. As you move the handle just past the center point, a spring in the switch will try to pull the handle all the way over, ensuring that the switch ends up in a definite ON or OFF state.
The diagram above shows a hysteresis 'loop' that describes how a comparator functions. The horizontal 'X' axis is the input, and represents the difference of the two input voltages. The vertical "Y" axis represents the comparator's output state. If the comparator is initially 'OFF', the MINUS input voltage has to become slightly above the PLUS input voltage before the comparator output turns 'ON'. This is represented by moving right along the bottom part of the loop.

Once the comparator is 'ON', the MINUS input voltage needs to drop slightly below the PLUS input voltage before it turns 'OFF' again (moving left along the top of the loop). The width of the loop outlined by an off-on-off cycle is the input hysteresis voltage. The hysteresis voltage for most comparators is in the millivolt range and usually only affects circuits where the input voltage rises or falls very slowly or has voltage spikes known as "noise".

The hysteresis voltage range can be increased if needed to help when the input voltage is noisy so that the output does not change states unnecessarily. The FLIP-FLOP circuits shown later on this page make use of an exaggerated hysteresis to create the memory effect.
Comparators with Open Collector outputs such as the LM339 or LM393 must be configured so that both outputs are HIGH when the voltage is within the desired limits. The voltage drop across the comparators output transistor has been ignored in the above calculations.

**Figure 10. Increasing The Input Hysteresis Range**

Comparators with Open Collector outputs such as the LM339 or LM393 must be configured so that both outputs are HIGH when the voltage is within the desired limits. The
LM311 comparator can have other output arrangements as it has both an open collector and open emitter on the output transistor.

**Converter Architectures**

An overwhelming variety of ADCs exist on the market today, with differing resolutions, bandwidths, accuracies, architectures, packaging, power requirements, and temperature ranges, as well as hosts of specifications, covering a broad range of performance needs. And indeed, there exists a variety of applications in data-acquisition, communications, instrumentation, and interfacing for signal processing, all having a host of differing requirements.

Considering architectures, for some applications just about any architecture could work well; for others, there is a "best choice". In some cases the choice is simple because there is a clear-cut advantage to using one architecture over another. For example, pipelined converters are most popular for applications requiring a throughput rate of more than 5 MSPS with good resolution. Sigma-delta converters are usually the best choice when very high resolution (20 bits or more) is needed. But in some cases the choice is more subtle. For example, the sigma-delta AD7722 and the successive-approximations AD974 have similar resolution (16 bits) and throughput performance (200 kmps). Yet the differences in their underlying architectures make one or the other a better choice, depending on the application.

The most popular ADC architectures available today are successive approximations (sometimes called SAR because a successive-approximations (shift) register is the key defining element), flash (all decisions made simultaneously), pipelined (with multiple flash stages), and sigma-delta (SD), a charge-balancing type. All A/D converters require one or more steps involving comparison of an input signal with a reference. Figure 1 shows qualitatively how flash, pipelined, and SAR architectures differ with respect to the number of comparators used vs. the number of comparison cycles needed to perform a conversion.

**Flash Converters**

Conceptually, the flash architecture (illustrated in Figure 2) is quite straightforward: a set of 2n-1 comparators are used to directly measure an analog signal to a resolution of n bits. For a 4-bit flash ADC, the analog input is fed into 15 comparators, each of which is biased to compare the input to a discrete transition value. These values are spaced one least-significant bit (LSB=FS/2n) apart. The comparator outputs simultaneously present 2n-1 discrete digital output states. If for example the input is just above ¼ of full scale, all comparators biased to less than ¼ full scale will output a digital ‘1’, and the others will output a digital ‘0’. Together, these outputs can be read much like a thermometer. The final step is to level-decode the result into binary form.

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Design Considerations and Implications: The flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle. The disadvantage of this approach is that it requires a large number of comparators that are carefully matched and properly biased to ensure that the results are linear. Since the number of comparators needed for an $n$-bit resolution ADC is equal to $2^n - 1$, limits of physical integration and input loading keep the
maximum resolution fairly low. For example, a 4-bit ADC requires 15 comparators, an 8-bit ADC requires 255 comparators, and a 16-bit ADC would require 65,535 comparators!

**Pipelined Architecture**

The pipelined (or pipelined-flash) architecture effectively overcomes the limitations of the flash architecture. A pipelined converter divides the conversion task into several consecutive stages. Each of these stages, as shown in figure 3, consists of a sample and hold circuit, an m-bit ADC (e.g. a flash converter), and an m-bit D/A converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The m-bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bits of the digital output. This same digital output is fed into an m-bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution. In principle, a pipelined converter with p pipelined stages, each with an m-bit flash converter, can produce a high-speed ADC with a resolution of n = p*m bits using p*(2^m-1) comparators. For example, a 2-stage pipelined converter with 8-bit resolution requires 30 comparators, and a 4-stage 16-bit ADC requires only 60 comparators. In practice, however, a few additional bits are generated to provide for error correction. For more about pipelined ADCs, click [here](#).

![Figure 3. A single pipelined converter stage.](image)

*Design Considerations and Implications:* Pipelined converters achieve higher resolutions than flash converters containing a similar number of comparators. This comes at the price of increasing the total conversion time from one cycle to p cycles. But since each stage samples and holds its input, p conversions can be underway simultaneously. The total throughput can therefore be equal to the throughput of a flash converter, i.e. one conversion per cycle. The difference is that for the pipelined converter, we have now introduced latency equal to p cycles. Another limitation of the pipelined architecture is that the conversion process generally requires a clock with a fixed period. Converting rapidly varying non-periodic signals on a traditional pipelined converter can be difficult because the pipeline typically runs at a periodic rate.
Successive Approximations

The successive-approximations architecture can be thought of as being at the other end of the spectrum from the flash architecture. While a flash converter uses many comparators to convert in a single cycle; a SAR converter, shown in figure 4, conceptually uses a single comparator over many cycles to make its conversion. The SAR converter works like an old-fashioned balance scale. On one side of the scale, we place the sampled unknown quantity. On the other side, we place a weight (generated by the SAR and DAC) that has the value of ½ of full-scale and compare the two values. This first weight represents the most significant bit (MSB). If the unknown quantity is larger, the ½-scale weight is retained; if the unknown quantity is smaller, it is removed. This series of steps is repeated n times, using successively smaller weights in binary progression (e.g., 1/4, 1/8, 1/16, 1/32, … 1/2^n of full scale) until the desired resolution, n, is attained. Each weight represents a binary bit, with the largest representing the most significant bit, and the smallest representing the least significant bit.

Figure 4. Successive-approximations architecture.

Design Considerations and Implications: A SAR converter can use a single comparator to realize a high resolution ADC. But it requires n comparison cycles to achieve n-bit resolution, compared to p cycles for a pipelined converter and 1 cycle for a flash converter. Since a successive-approximations converter uses a fairly simple architecture employing a single SAR, comparator, and DAC, and the conversion is not complete until all weights have been tested, only one conversion is processed during n comparison cycles. For this reason, SAR converters are more often used at lower speeds in higher-resolution applications. SAR converters are also well suited for applications that have non-periodic inputs, since conversions can be started at will. This feature makes the SAR architecture ideal for converting a series of time-independent signals. A single SAR converter and an input multiplexer are typically less expensive to implement than several sigma-delta converters. With dither noise present, SAR and pipelined converters can use averaging to increase the effective resolution of the converter: for every doubling of sample rate, the effective resolution improves by 3 dB or ½ bit.

One consideration when using a SAR or pipelined converter is aliasing. The process of sampling a signal leads to aliasing - the frequency-domain reflection of signals about the sampling frequency. In most applications, aliasing is an unwanted effect that requires a low-pass anti-alias filter ahead of the ADC to remove high-frequency noise components, which would be aliased into the pass band. However, under sampling can put aliasing to good use, most often in communications applications, to convert a high-frequency signal to a lower frequency. Under sampling is effective as long as the total bandwidth of a signal meets the Nyquist criterion (less than one-half the sampling rate), and the converter has sufficient acquisition and signal sampling performance at the higher frequencies where the signal resides. While fast SAR converters are capable of under sampling, the faster pipelined converters tend to be more effective at it.
**Sigma-Delta**

The sigma-delta architecture takes a fundamentally different approach from those outlined above. In its most basic form, a sigma-delta converter consists of an integrator, a comparator, and a single-bit DAC, as shown in Figure 5. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the DAC, and the DAC's output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "over sampled" rate. The digital data coming from the ADC is a stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output. For more about sigma-delta conversion, click here.

![Figure 5. Sigma-delta ADC architecture.](image)

**Design Considerations and Implications:** One of the most advantageous features of the sigma-delta architecture is the capability of noise shaping, a phenomenon by which much of the low-frequency noise is effectively pushed up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low-bandwidth high resolution ADCs for precision measurement. Also, since the input is sampled at a high "over sampled" rate, unlike the other architectures described in this paper, the requirement for external anti-alias filtering is greatly reduced. A limitation of this architecture is its latency, which is substantially greater than that of the other types. Because of over sampling and latency, sigma-delta converters are not often used in multiplexed signal applications. To avoid interference between multiplexed signals, a delay at least equal to the decimator's total delay must occur between conversions. These characteristics can be improved in sophisticated sigma-delta ADC designs by using multiple integrator stages and/or multi-bit DACs.

References: [http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma.html](http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma.html)
Pulse width modulation has been described as a poor man's digital to analog converter but in reality, it is one of the most power efficient ways to amplify a signal. PWM is also sometimes referred to as class D amplification. The modulation signal is used to turn on and off the output signal. The carrier signal as shown in Figure 11 is a saw tooth wave. The output is created by setting the output high when the modulation signal is greater than the carrier signal. The resulting PWM signal is shown in Figure 12. The PWM signal has a 50% duty cycle when the modulation signal is approximately half voltage.

![PWM Modulation](image)

**Figure 11. Pulse width modulated signal**

![Modulation Output](image)

**Figure 12. Graphical plot of a PWM modulated signal.**

PWM is truly a form of modulation used in communications theory because the modulating signal is translated as shown in Figure 13. One knowledgeable in communications theory recognizes that the sidebands on each side of the carrier frequency are in the same form as

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5 Class D amplifier Design: [http://sound.westhost.com/articles/pwm.htm](http://sound.westhost.com/articles/pwm.htm)
an amplitude modulated (AM) signal. The carrier frequency is the inverse of the period of the PWM period. The more narrow the on or off periods, the higher the modulation frequency becomes. Figure 13 also shows a sideband just above zero Hz. This is the spectrum of the original modulation signal. Filtering this side band from all of the higher sidebands will result in reconstructing the original modulating signal except that the power can be greatly increased.

**Figure 13. Frequency spectrum for PWM signal**

Amplification takes place by using power transistors to switch the high voltages to the load. Since transistors dissipate little power when they completely turned on or off, the amplifiers has low losses hence very good efficiency. The issue is how to create effective power filters to remove the higher sidebands and carrier signals? For our application (and audio signals in general) the unwanted signals are simply rejected by the system receiving the signal because the device being driven cannot respond the higher frequency signals. Other applications require some kind of analog filtering as shown in Figure 14. Comparing Figure 13 and Figure 14, one will see that the signal around zero Hz is not attenuated whereas the higher sidebands and carrier signals are greatly reduced.
Figure 14. Spectrum after filtering with a 4th Order Butterworth Filter
The effects of filtering are shown in Figure 15 through **Error! Reference source not found.**. Again, it can be seen that the amplitude of the original signal remains approximately unchanged while the distortion and apparent noise generated by the PWM are greatly reduced.

Figure 15. Unfiltered reconstructed signal
Figure 16. Spectrum of unfiltered reconstructed signal

Figure 17. Filtered reconstructed signal