

---

```
-- Company: University of Idaho
-- Engineer: Greg Donohoe
--
-- Create Date: 15:17:23 02/06/2008
-- Design Name: Simple2
-- Module Name: simple2 - Behavioral
-- Description: VHDL demo with internal signal nodes
--
```

---

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
entity simple2 is
    Port ( A, B, C : in STD_LOGIC;
           Y : out STD_LOGIC);
end simple2;
```

```
architecture Behave of simple is
    signal N1, N2: STD_LOGIC;
begin
    N1 <= A and B;
    N2 <= not C;
    Y <= N1 or N2;
end Behave;
```