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-- VHDL example 3 with conditional assignments
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```

```
library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
entity lab6a is
```

```
    port (a2, a1, a0: in std_logic;
```

```
          y: out std_logic);
```

```
end lab6a;
```

```
architecture demo of lab6a is
```

```
begin
```

```
    y <= '1' when ((a2 = '0' and a1 = '0' and a0 = '1') or
```

```
                  (a2 = '0' and a1 = '1' and a0 = '1') or
```

```
                  (a2 = '1' and a1 = '0' and a0 = '0') or
```

```
                  (a2 = '1' and a1 = '1' and a0 = '0')) else '0';
```

```
end demo;
```

```
-- VHDL example 4 with conditional assignments
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```
-- using vectors to represent minterms
```

```
library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
entity lab6b is
```

```
    port (a: in std_logic_vector(2 downto 0);
```

```
          y: out std_logic);
```

```
end lab6b;
```

```
architecture demo of lab6b is
```

```
begin
```

```
    y <= '1' when (a = "001" or a = "010" or a = "100" or a = "110") else '0';
```

```
end demo;
```