

Homework #5: Due Friday Mar 21

Goal: Practice designing sequential circuit with combinational logic blocks and load enable.

10 points. Design a 4-bit counter using a ripple-carry adder. Use the equations in Figure 5.3.1 in the Harris & Harris text for the outputs S (sum) and C_{out} (carry out). Implement the full adder with gates from the tables below. The counter should reset to zero when the reset signal is active (**reset=1**). The counter should count up when the count-enable is active (**count_en=1**) and hold the previous count when **count_en = 0**.

Gate	$t_{pd}(ps)$	$t_{cd}(ps)$
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40

Gate	$t_{setup}(ps)$	$t_{hold}(ps)$	$t_{ccq}(ps)$
D flip-flop with enable and synchronous reset	30	0	25

Draw your design and determine the fastest clock rate at which the counter can operate.

Hint: you will first have to perform static timing analysis on your full adder, then determine the maximum delay through the ripple-carry adder. There is not carry into or out of the counter.