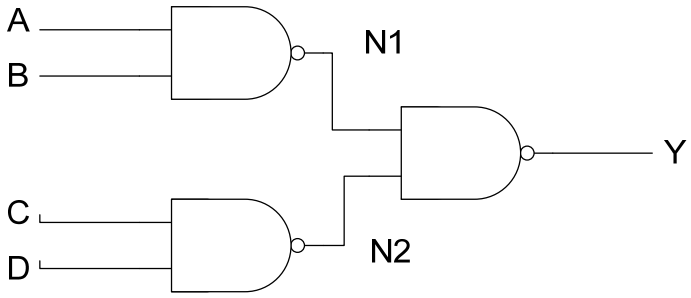
Structural VHDL Example

The code samples below implement the logic function Y=AB+CD, using three 2-input NAND gates, as shown below, in structural VHDL. 'NAND2.vhd' and 'struct_gates.vhd' are two separate files in the same project.




```
-- NAND2.vhd Two-input NAND gate

library ieee;
use ieee.std_logic_1164.all;

entity NAND2 is
   port (In0, In1: in std_logic;
            F: out std_logic);
end NAND2;

architecture Behave of NAND2 is
begin
   F <= not (In0 and In1);
end Behave;
```

```
-- struct_gates.vhd
--
-- Structural VHDL example
-- Implements Y = AB + CD using three 2-input NAND gates

library ieee;
use ieee.std_logic_1164.all;

entity struct_gates is
  port (A,B,C,D: in std_logic;
        Y: out std_logic);
end struct_gates;

architecture struct of struct_gates is
   signal N1, N2: std_logic;

   component NAND2
      port (In0, In1: in std_logic;
                  F: out std_logic);
   end component;

 begin

  u1: NAND2 port map (A, B, N1);
  u2: NAND2 port map (C, D, N2);
  u3: NAND2 port map (N1, N2, Y);

end struct;
```