ECE440 Spring 2004

RTL Design Example 20 Feb 04

Specification: Unsigned Averager

Design a circuit to compute the sample mean of a string of eight 8-bit, unsigned integers. The output is also 8 bits.

The equation for the sample mean is:

$$\bar{x} = \frac{1}{N}\sum_{i=1}^{N} x_i$$

Where $\{x_i\}$ are the input samples and N is the sample size. In our case N=8, so:

$$\bar{x} = \frac{1}{8}\sum_{i=1}^{8} x_i \text{ or equivalently } \bar{x} = \frac{1}{8}\sum_{i=0}^{7} x_i$$

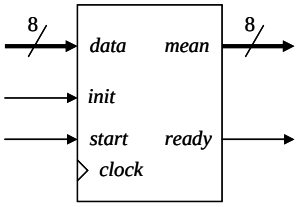
Specifications:

inputs

data	8-bit data input vector, non-negative integer
start	control signal to start computation
init	control signal to initialize module

outputs

mean	8-bit data output vector, non-negative integer
ready	status signal: module is ready to start a new computation



Before use, the module must be initialized by asserting the init signal for one clock period (rising edge to rising edge). When the module is ready to start a computing sequence, it asserts *ready* and waits for the *start* signal to be asserted. The start signal should last at least one clock cycle. On receiving a *start* signal, the module de-asserts *ready*. On the first falling clock edge after the clock period containing the *start* signal, the module expects the first data sample to be stable at the *data* input. On this, and each subsequent falling edge, the averager latches a data sample. When eight samples have been read, the module completes the computation, and latches an 8-bit output.

The module then reasserts *ready*, and waits for the *start* signal to begin the next computational sequence. The last mean value is retained at the output until a new one is ready.