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-- Simple 4-bit counter

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Xilinx primitive components.
library UNISIM;
use UNISIM.VComponents.all;

entity counter is
port (D: in std_logic_vector(3 downto 0);
      clock, clear, load, count_enable: in std_logic;
      count: buffer std_logic_vector(3 downto 0));
end counter;

architecture Behavioral of counter is
begin
  process (clock, clear, load, count_enable)
  begin
    if rising_edge(clock) then
      if (clear='1') then
        count <= "0000";
      else
        if (load = '1') then
          count <= D;
        else
          if (count_enable = '1') then
            count <= count + 1;
          end if;
        end if;
      end if;
    end if;
  end process;

end Behavioral;

```