

ECE440 Digital Systems Engineering

Spring 2005 Homework #3

Due Date

On campus students: Friday Feb 11

Off campus students: Friday Feb 25

Goals: Understand how to write and use a basic testbench in VHDL. Be able to read test vectors and reference vectors from a file, impose test patterns on the Unit Under Test (UUT), compare with reference vectors, and report discrepancies using the ASSERT statement.

Assignment

You may work in pairs. Be sure to put both names on the report that you turn in.

Create a VHDL testbench to test your four-bit adder with carry (Part 2 of Assignment #2.) Use the Multiplexer and Multiplexer Testbench models handed out in class (available under Lecture #10 on the class web page), as a template. Use your adder instead of the 'mux2' module instantiated as the Unit Under Test (UUT) in the example.

Your testbench should read test vectors and reference vectors from a file, present the test signal to your adder, and compare the output from your adder with the reference vectors. If the two do not agree, your testbench program should report an error with an ASSERT statement.

Include at least one 'Seeded' error, to ensure that your testbench is able to detect and report errors.

Simulate your design in ModelSim. (You simulate the testbench, not the adder.) Look at the waveform plot to verify that it's working correctly.

Notes:

1. The FILE IO use in the text and in our examples use VHDL 1987 syntax. ModelSim-XE V. 5.8c uses VHDL 2002 file syntax by default. When you compile the older-style code, you might get a compiler warning, but the compiler is smart enough to do the right thing, and your design should simulate correctly. You can choose which version of VHDL you use -- 1987, 1993, or 2002 -- by right-clicking on the VHDL file name in the Workspace Project window, selecting Compile, then Compile Properties, and you will see a list of options.

2. The 'run' command in ModelSim will simulate for a fixed period of time, typically 100 ns. To run to the end of your testbench, type:

```
SIM> run -all
```

Turn In

The source code for your testbench, and your test vector file. Include a brief report describing your program and interpreting the results that you observe.