

Kenneth Joseph Hass

Electrical and Computer Engineering
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EDUCATION

- May 2007 Ph.D. Electrical Engineering, University of Idaho (with coursework from the University of New Mexico). Dissertation research on design of embedded memory circuits using magnetic tunnel junctions.
- August 1979 M.S. Electrical Engineering, Kansas State University. Thesis research on a microprocessor system for real-time digital signal processing.
- May 1978 B.S. Electrical Engineering, Kansas State University

TEACHING EXPERIENCE

- 2007-present Research Associate Professor, Electrical and Computer Engineering, University of Idaho. Courses taught include:
- Pulse and Digital Circuits
 - Semiconductor Memory Circuits (new course)

RESEARCH EXPERIENCE

- 2002-2007 Senior Research Engineer, Center for Advanced Microelectronics and Biomolecular Research, University of Idaho
- Research and development of radiation-tolerant CMOS integrated circuits
 - Project leader for creation of radiation-tolerant standard cell libraries in 0.25 μ m and 0.18 μ m CMOS, responsible for design, fabrication and characterization
 - Project leader for physical design of a field-programmable processor array
 - Lead designer for embedded magnetic memory circuits.
- 1996-2002 Senior Research Engineer, Microelectronics Research Center, University of New Mexico
- Research and development of radiation-tolerant and ultra-low-power CMOS circuit designs
 - Project leader for high-speed ultra-low power correlators
 - Project leader for Single-Event Effects testing, including development of instrumentation and test automation
- 1983-1996 Distinguished Member of Technical Staff, Microelectronics Directorate, Sandia National Laboratories
- Design of radiation-hardened CMOS microelectronics, including full-custom processors and memories, gate-arrays, and Field Programmable Gate Arrays
 - Project leader for GPS encryption module integrated circuit
 - Member of design teams for 32-bit microprocessor, floating-point coprocessor, 8-bit microcontroller, and various application-specific integrated circuits
 - Top-secret 'Q' clearance
- 1979-1983 Member of Technical Staff, Safeguards Directorate, Sandia National Laboratories

- Hardware and software design for microprocessor-based real-time systems
- Project leader for upgrade to Army Facility Intrusion Detection System (FIDS)
- Modeling and implementation of embedded seismic DSP software
- Design of instrumentation for field testing

PUBLICATIONS

K.J. Hass, G.W. Donohoe, Y.-K. Hong and B. C. Choi, **Magnetic Flip Flops for Space Applications**, *IEEE Transactions on Magnetics*, vol. 42, no. 10, pp. 2751-2753, Oct. 2006.

B. C. Choi, Q. F. Xiao, Y. K. Hong, S. H. Gee, J. Jabal, H. Han, K. J. Hass, and G. W. Donohoe, **Numerical simulation study of magnetization precession dynamics in submicrometer elliptical Ni₈₀Fe₂₀ thin-film elements**, *IEEE Transactions on Magnetics*, vol. 42, no. 10, pp. 3216-3218, Oct. 2006.

Jeffrey R. Piepmeier and K. Joseph Hass, **Ultralow-Power Digital Correlator for Microwave Polarimetry**, *NASA Tech Briefs*, pp. 36-37, August 2004.

F. W. Sexton, R. K. Treece, K. J. Hass, K. L. Hughes, G. L. Hash, C. L. Axness, S. P. Buchner and K. Kang, **SEU Characterization and Design Dependence of the SA3300 Microprocessor**, *IEEE Transactions on Nuclear Science*, 37(6):1861-1868, December 1990.

K. J. Hass, R. K. Treece and A. E. Giddings, **A Radiation-Hardened 16/32-Bit Microprocessor**, *IEEE Transactions on Nuclear Science*, 36(6):2252-2257, December 1989.

K. J. Hass, **A Minimal Microcomputer System Based On The SBP9900A**, *Sandia Laboratories Technical Report SAND79-1970*, July 20, 1979.

K. J. Hass, D. H. Lenhert and N. Ahmed, **On A Microcomputer Implementation of an Intrusion-Detection Algorithm**, *IEEE Transactions on Acoustics, Speech and Signal Processing*, ASSP-27(6):782-789, December 1979.

CONFERENCE PAPERS

William Walker, Gregory Donohoe, David Buehler, Joe Hass, Chris Canine, and Pen-Shu Yeh, **The Field Programmable Processor Array: Design and Testing**, *13th NASA Symposium on VLSI Design*, May 5-6, 2007.

K. J. Hass, G. Donohoe, Y.-K. Hong, B.-C. Choi, K. DeGregorio and R. Hayhurst, **Integrated Magnetic Memory for Embedded Computing Systems**, *IEEE Aerospace Conference*, Big Sky, MT, March 5-9, 2007.

K. J. Hass, G. Donohoe, Y.-K. Hong, B.-C. Choi, K. DeGregorio and R. Hayhurst, **Magnetic Shadow RAM**, *IEEE Non-Volatile Memory Technology Symposium*, San Mateo, CA, November 5-8, 2006.

J. Jabal, Y. Hong, H. Han, S. Gee, B. Choi, G. Abo, J. Hass and G. Donohoe, **Lateral Size Dependence of Pac-man shaped Ni₈₀Fe₂₀ Element on Magnetization Reversal**, *IEEE International Magnetics Conference*, May 8-12, 2006.

B. Choi, Q. Xiao, Y. Hong, S. Gee, J. Jabal, H. Han, K. Hass and G. Donohoe, **Numerical Simulation Study of Magnetization Precession Dynamics in Submicron Elliptical Ni₈₀Fe₂₀ Thin Film Elements**, *IEEE International Magnetics Conference*, May 8-12, 2006.

K.J. Hass, G.W. Donohoe, Y. Hong and B. Choi, **Magnetic Latches for Space Applications**, *IEEE International Magnetics Conference*, May 8-12, 2006.

K. J. Hass, G. W. Donohoe and Y.-K. Hong, **SEU-Resistant Magnetic Flip Flops**, *12th NASA Symposium on VLSI Design*, October 2005.

- J. Gambles, L. Miles, J. Hass, W. Smith, S. Whitaker and B. Smith, **An Ultra-Low-Power, Radiation-Tolerant Reed Solomon Encoder for Space Applications**, *IEEE Custom Integrated Circuits Conference*, September 2003.
- K. Joseph Hass and Jeffrey R. Piepmeier, **An Ultra-Low Power, Radiation Tolerant, High Speed Correlator**, *11th NASA Symposium on VLSI Design*, May 2003.
- Jody W. Gambles, Kenneth J. Hass and Sterling R. Whitaker, **Radiation Hardness of Ultra Low Power CMOS VLSI**, *11th NASA Symposium on VLSI Design*, May 2003.
- K. E. Li, M. A. Xapsos, C. Poivey, R. F. Stone, P-S. Yeh, J. Gambles, J. Hass, G. Maki and J. Murguia, **Qualification of an Ultra-Low Power Reed Solomon Encoder for NASA's Space Technology 5 Mission**, *HEART Conference*, March, 2003.
- Brian Smith, K. Joe Hass and James Murguia, **Development of a Low Power Digital Signal Processor**, *10th NASA Symposium on VLSI Design*, 9.2.1-9.2.9, March 2002.
- L. Miles, J. Venbrux, J. Gambles, J. Hass, W. Smith, G. Maki and S. Whitaker, **An Ultra-Low-Power, Radiation-Tolerant Data/Image Compressor for Space Applications**, *10th NASA Symposium on VLSI Design*, 9.3.1-9.3.7, March 2002.
- Harry F. Benz, Jody W. Gambles, Sterling R. Whitaker, Kenneth J. Hass, Pen-Shu Yeh and Gary K. Maki, **Low Power Radiation Tolerant VLSI for Advanced Spacecraft**, *IEEE Aerospace Conference*, March 2002.
- J. Piepmeier and J. Hass, **Ultra-low Power Digital Correlator for Passive Microwave Polarimetry**, *NASA Earth Science Technology Conference*, August 30, 2001.
- K. Joseph Hass, Jack Venbrux and Prakash Bhatia, **Logic Design Considerations for 0.5-Volt CMOS**, *2001 Conference on Advanced Research in VLSI*, 75-85, March 14-16, 2001.
- K. Joe Hass and David F. Cox, **Level Shifting Interfaces for Low Voltage Logic**, *9th NASA Symposium on VLSI Design*, 3.1.1-3.1.7, November 2000.
- S. Whitaker, J. Hass, L. Davis, L. Arave, K. Arave and L. Miles, **Ultra-Low Power CCSDS Encoder**, *9th NASA Symposium on VLSI Design*, 3.5.1-3.5.7, November 2000.
- K. Joe Hass and Harry C. Shaw, **Cryogenic Operation of Ultra Low Power CMOS**, *9th NASA Symposium on VLSI Design*, 3.4.1-3.4.7, November 2000.
- Gregory W. Donohoe, K. Joseph Hass, Stephen Bruder and Pen-Shu Yeh, **A Reconfigurable Data Path Processor for Space Applications**, *Proc. Military and Aerospace Applications of Programmable Logic Devices 2000*, Laurel, MD, September 24-28, 2000.
- K. Joe Hass, **Probabilistic Estimates of Upset Caused by Single Event Transients**, *8th NASA Symposium on VLSI Design*, 4.3.1-4.3.9, October 1999.
- Gregory W. Donohoe and K. Joseph Hass, **Reconfigurable Data Path Processor for Space Applications**, *8th NASA Symposium on VLSI Design*, 2.2.1-2.2.8, October 1999.
- K. J. Hass and J. W. Gambles **Single Event Transients in Deep Submicron CMOS**, *42nd Midwest Symposium on Circuits and Systems*, August 1999.
- K. J. Hass and J. W. Gambles, **Mitigating Single Event Upsets from Combinational Logic**, *7th NASA Symposium on VLSI Design*, 4.1.1-4.1.10, October 1998.
- K. J. Hass and D. F. Cox, **Transform Processing on a Reconfigurable Data Path Processor**, *7th NASA Symposium on VLSI Design*, 7.4.1-7.4.12, October 1998.

CONFERENCE PRESENTATIONS

- Integrated Magnetic Memory for Embedded Computing Systems**, *IEEE Aerospace Conference*, Big Sky, MT, March 2007 (scheduled).

Magnetic Shadow RAM, *IEEE Non-Volatile Memory Technology Symposium*, San Mateo, CA, November 6, 2006.

Magnetic Latches for Space Applications, *IEEE International Magnetics Conference*, San Diego, CA, May 12, 2006.

SEU-Resistant Magnetic Flip Flops, *12th NASA Symposium on VLSI Design*, Coeur d'Alene, ID, October 2005.

An Ultra-Low Power, Radiation Tolerant, High Speed Correlator, *11th NASA Symposium on VLSI Design*, Coeur d'Alene, ID, May 2003.

Logic Design Considerations for 0.5-Volt CMOS, *2001 Conference on Advanced Research in VLSI*, Salt Lake City, UT, March 15, 2001.

Cryogenic Operation of Ultra Low Power CMOS, *9th NASA Symposium on VLSI Design*, Albuquerque, NM, November 2000.

Level Shifting Interfaces for Low Voltage Logic, *9th NASA Symposium on VLSI Design*, Albuquerque, NM, November 2000.

Probabilistic Estimates of Upset Caused by Single Event Transients, *8th NASA Symposium on VLSI Design*, Albuquerque, NM, October 1999.

Single Event Transients in Deep Submicron CMOS, *42nd Midwest Symposium on Circuits and Systems*, Las Cruces, NM, August 1999.

Transform Processing on a Reconfigurable Data Path Processor, *7th NASA Symposium on VLSI Design*, Albuquerque, NM, October 1998.

Mitigating Single Event Upsets from Combinational Logic, *7th NASA Symposium on VLSI Design*, Albuquerque, NM, October 1998.

A Radiation-Hardened 16/32-Bit Microprocessor, *IEEE Nuclear and Space Radiation Effects Conference*, Marco Island, FL, July 27, 1989.

SEMINAR/WORKSHOP PRESENTATIONS

Embedded Magnetic Memory, *Boise State University Research Overview*, Boise, ID, September 15, 2006.

SEU-Resistant Magnetic Flip Flops, *University of Idaho ECE Graduate Seminar*, Moscow, ID, October 3, 2005.

Embedded MRAM Circuits, *Air Force Research Laboratory Project Review*, Albuquerque, NM, August 15, 2006.

Embedded MRAM Issues, *Air Force Research Laboratory Project Review*, Albuquerque, NM, August 20, 2004.

Mainstreaming RHBD, *DARPA RADHARD By Design Workshop*, Alexandria, VA, February 12, 2003.

LRR Correlator ASIC, *Critical Design Review*, Albuquerque, NM, June 13, 2002.

Radiation Tolerant and Ultra-Low Power CMOS, *University of Idaho ECE Graduate Seminar*, Moscow, ID, February 14, 2002.

Correlator Chip for the Lightweight Rainfall Radiometer, *Preliminary Design Review*, Albuquerque, NM, August 9, 2001.

500 MHz Cross Correlator Design Review, Albuquerque, NM, February 15, 2001.

PATENTS

Disclosure Kenneth J. Hass, **Magnetic Shadow RAM**, March 20, 2006.

Disclosure	Kenneth J. Hass, Radiation-Tolerant Magnetic Tunneling Junction Memory Cell , February 9, 2005.
6,731,158	Kenneth J. Hass, Self Regulating Body Bias Generator , May 4, 2004.
6,583,470	Gary K. Maki, Jody W. Gambles and Kenneth J. Hass, Radiation Tolerant Back Biased CMOS VLSI , June 24, 2003.
6,573,773	Gary Maki, Kenneth Hass, Shi Quan and James Murguia, Conflict Free Radiation Tolerant Storage Cell , June 3, 2003.
6,326,809	Jody W. Gambles, Kenneth J. Hass and Kelly B. Cameron, Apparatus For And Method Of Eliminating Single Event Upsets In Combinational Logic , December 4, 2001.

AWARDS

Sep 1, 2005	NASA Certificate of Recognition for the creative development of the Ultra-Low Power Digital Correlator for Passive Microwave Polarimetry
Nov 9, 1995	NAVSTAR/GPS SAASM Summit III Participation Award
Sep 1995	U.S. Air Force Global Positioning System Team Excellence Award
Mar 28, 1995	Sandia Award For Excellence for outstanding architectural and circuit design contributions to the successful SAASM proof-of-concept demonstration
Jan 26, 1995	NAVSTAR/GPS Certificate of Appreciation for outstanding contribution to the SAASM program
1992–1995	Annual Certificate of Appreciation for contribution to the Sandia Science Advisers Program (supporting elementary school science teachers)
Jun 13, 1991	Sandia Award For Excellence for contribution to the development of a radiation-hardened floating point unit
July 1990	Named a Distinguished Member of the Technical Staff at Sandia National Laboratories. DMTS is the highest level of the technical staff, awarded by nomination and management review, and limited to 10% of the population.
Feb 1, 1990	Sandia Award For Excellence for contribution to the development of a 16-bit radiation-hardened microprocessor
1978	Eta Kappa Nu Electrical Engineering Honorary Society and Tau Beta Pi Honor Society at Kansas State University