1. Consider the BUCK converter from problem 2 of homework set 1 (copied below for your convenience). Using software introduced in class, simulate enough switching cycles of this converter to bring its output to steady state. Use an ideal switch and a 40 \( \mu \text{F} \) capacitor. At a minimum, show the waveforms of the voltage across the capacitor and the current in the inductor.

2. A buck converter has a 12V input and a 5V, 100W output. Its MOSFET switches at 100kHz with a 50% duty cycle. The MOSFET has an “on resistance” of 50m\( \Omega \). The diode has an on-state voltage drop of 1.00V. Each device requires 100ns to switch on or off. Assume negligible current ripple in the inductor. Ignore diode reverse recovery. Estimate the total power loss and the energy efficiency of this converter.

3. During a diode’s reverse recovery, the forward voltage is relatively low. The diode cannot block until the charge is removed. Therefore, the diode apparently causes little power loss in the diode. However, this current must flow somewhere. Consider a buck converter where the diode is ideal except for a reverse recovery time of 100ns and a stored charge of 10\( \mu \text{C} \). The input voltage is 100V and the output voltage is 12V. The load is 120W. The transistor’s switching time is the same 100ns as the diode recovery time. Assume negligible current ripple in the inductor.

   a. What is the peak reverse recovery current in the diode?

   b. What is the power loss in the transistor due to diode reverse recovery?

4. A power semiconductor in a TO-220 package has a junction-to-case thermal resistance of 1.2K/W. Without a heat sink, it has a junction-to-ambient thermal resistance of 45K/W. If we want to keep the junction temperature below 150°C, what is the maximum power that can be dissipated from this power semiconductor?

   a. Without a heat sink?

   b. With a heat sink?

   c. Find a heat sink that allows 15 Watts dissipation for the temperature conditions described. Attach its data sheet and explain, with numbers from the data sheet, why you believe your selection will work.

Problem 2 from HW set 1
The buck converter having a switching power pole, as described in Figure 1.22 of the Mohan textbook, has an input of 50 Volts dc and an average output voltage of 25 Volts. The switching frequency is 500 kHz and the power to the load resistor is 125 Watts. Assume that the capacitance is large enough to ensure a negligible voltage ripple across the load resistance.
a. Determine the duty ratio.
b. Design the inductance necessary to limit the peak inductor current to 5.30 Amps.