University of Idaho

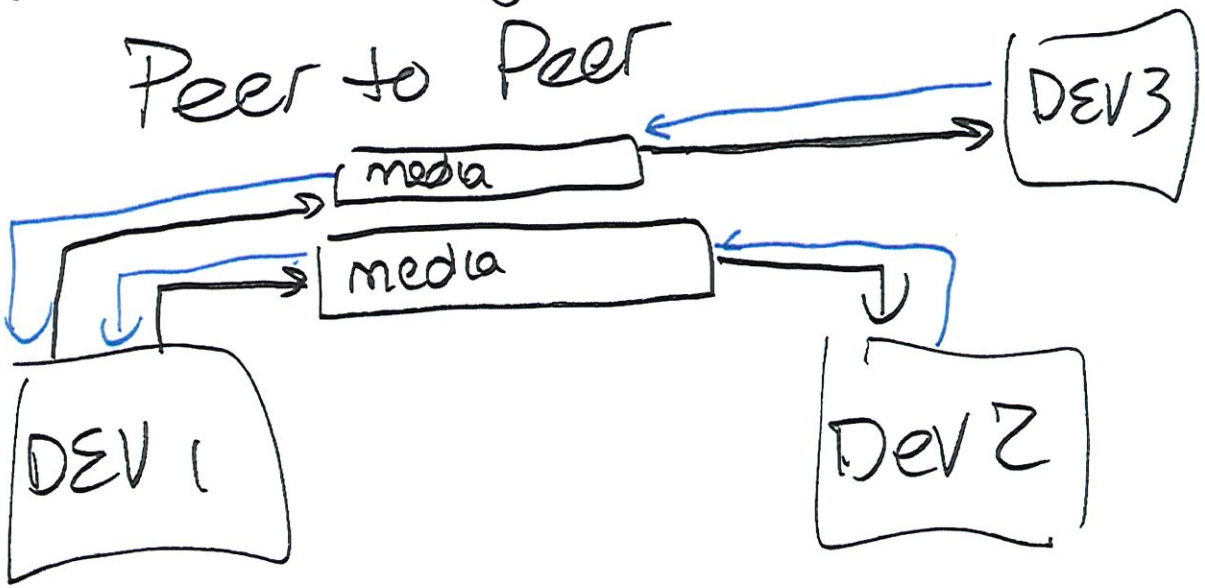
ECE 444 / ECE 544 / CS 444 / CS 544 Supervisory Control and Critical Infrastructure Systems

Session 13

~~L11 7/8~~ L13 1/13

Implementing ~~Architecture~~ Architecture

Peer to Peer

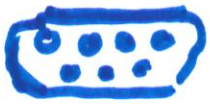


- sharing the channel
  - each device has access to send or receive → not simultaneously
- Duplex → simultaneous access { half, full

serial implementations

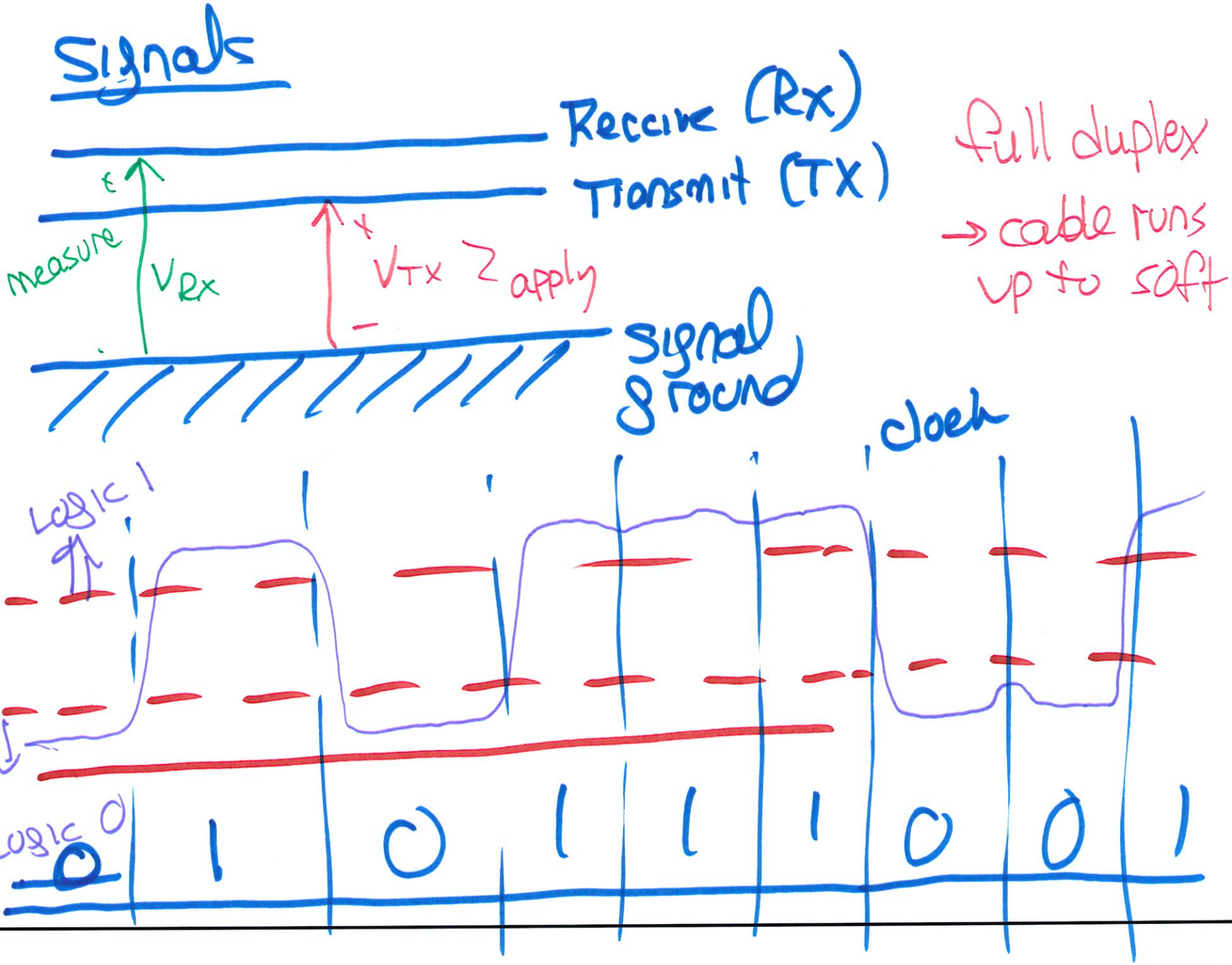
cable

- RS 232 → copper wire serial cable
  - Recommended standard → EIA or TIA 232
    - EIA → electronics industry Association
    - TIA → Telecom. Industry Associations
  - 232 – designates termination
  - → 7 pin or 15 pin



→ pin out defined by vendor

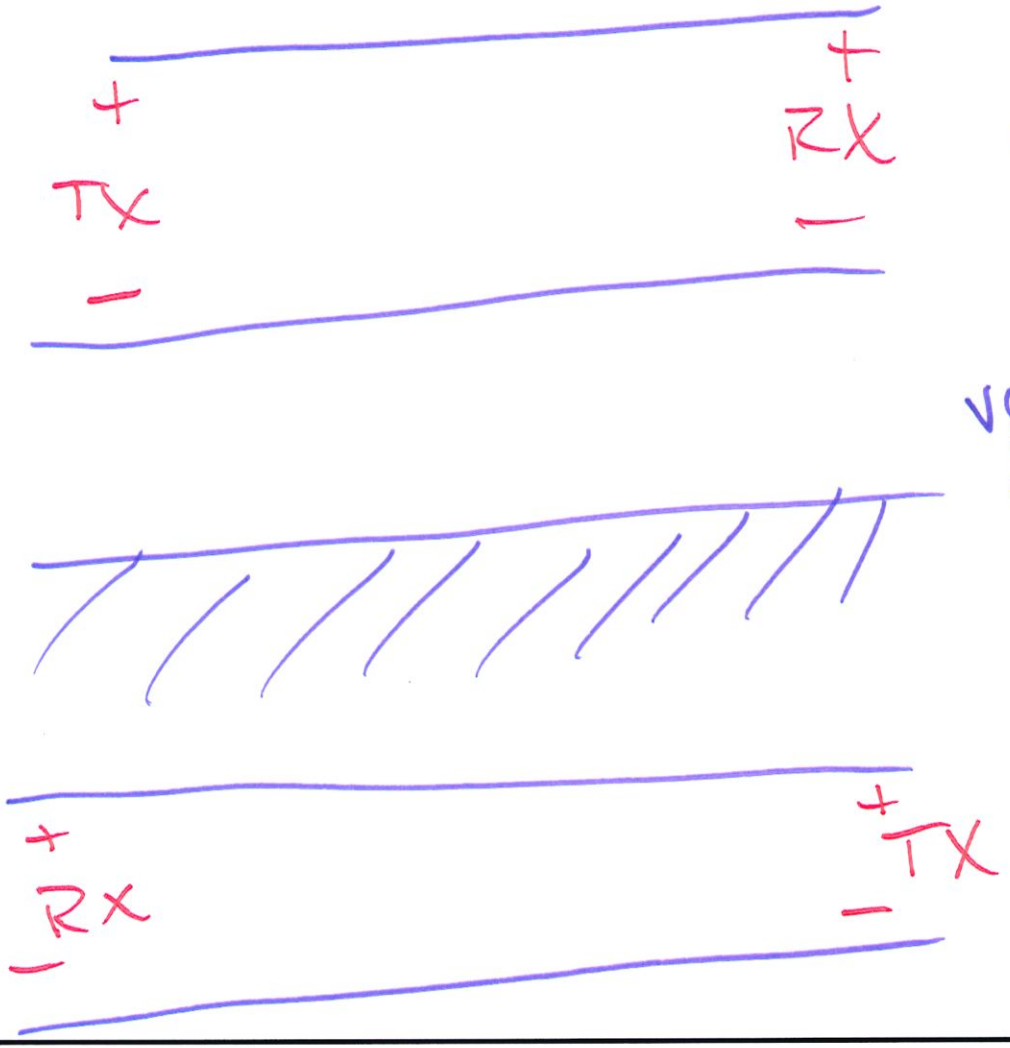
Signals


Receive (Rx)
Transmit (TX)
full duplex
→ cable runs up to 50ft
ε
measure
V_{Rx}
x
V_{TX} ≥ apply
signal ground
clock
Logic 1
Logic 0
0 1 0 1 1 1 0 0 1

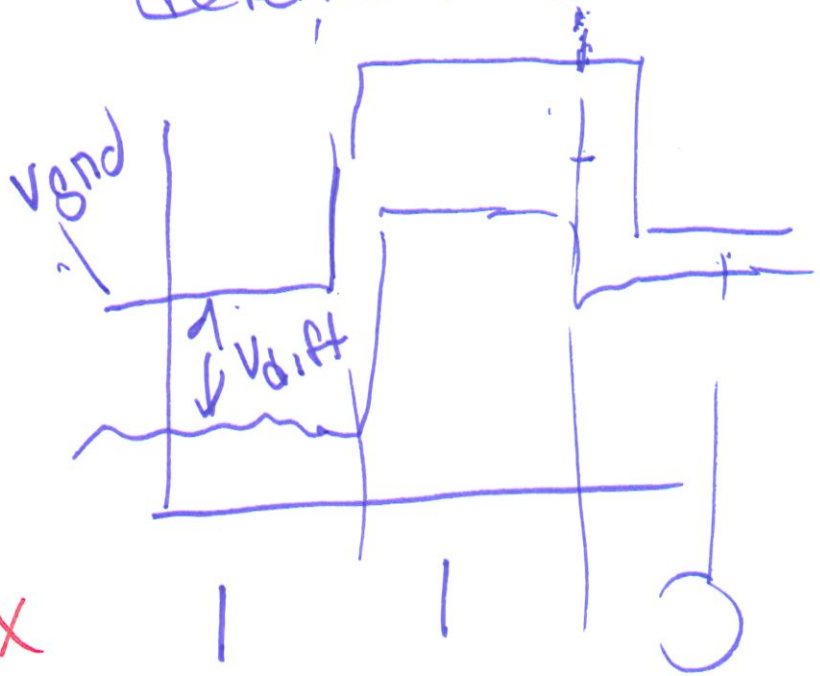
RS-485 → same connectors

→ differential signal - 4 wires for data

- 500 - 1500 ft



→ voltage difference determines logic level

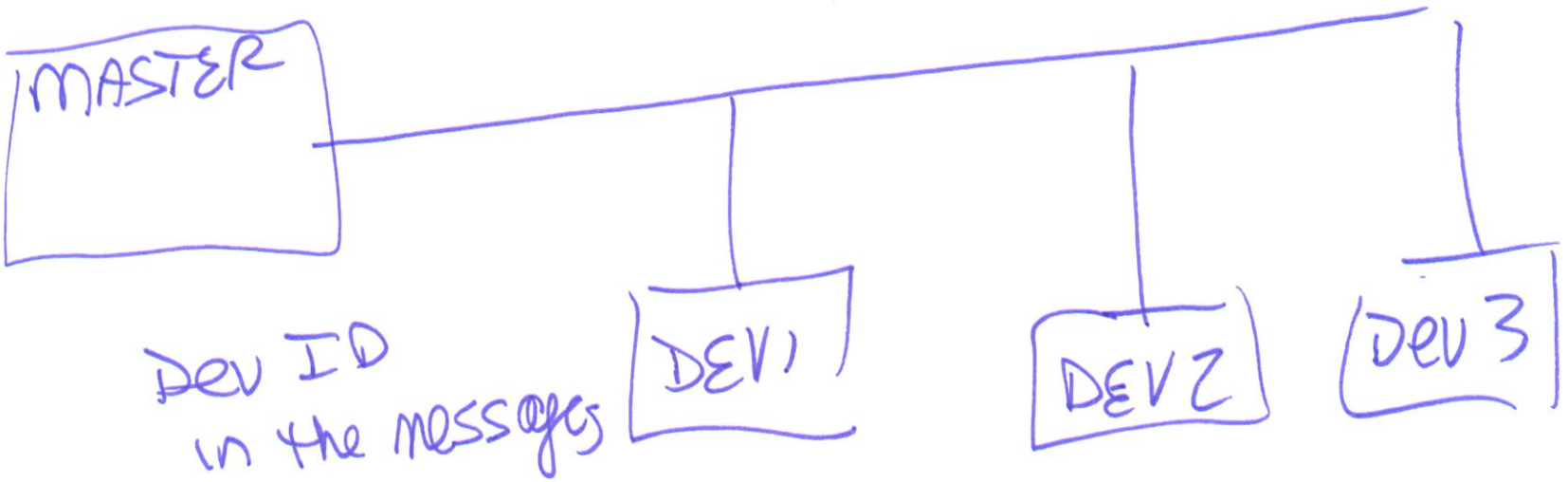


RS 485

also supports

multidrop → multicast
broadcast

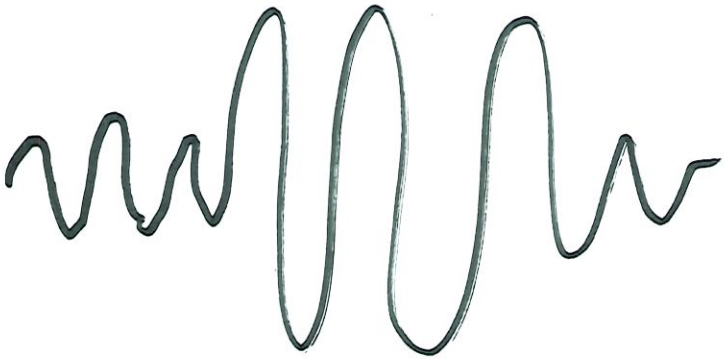
RS 232 - device to device



Analog transmission

Broadband

→ Analog signal encoded based on amplitude and/or frequency modulation or phase



→ mostly used in wireless transmission

→ undirected communication Media

→ long distance

Digital Transmission

→ Baseband

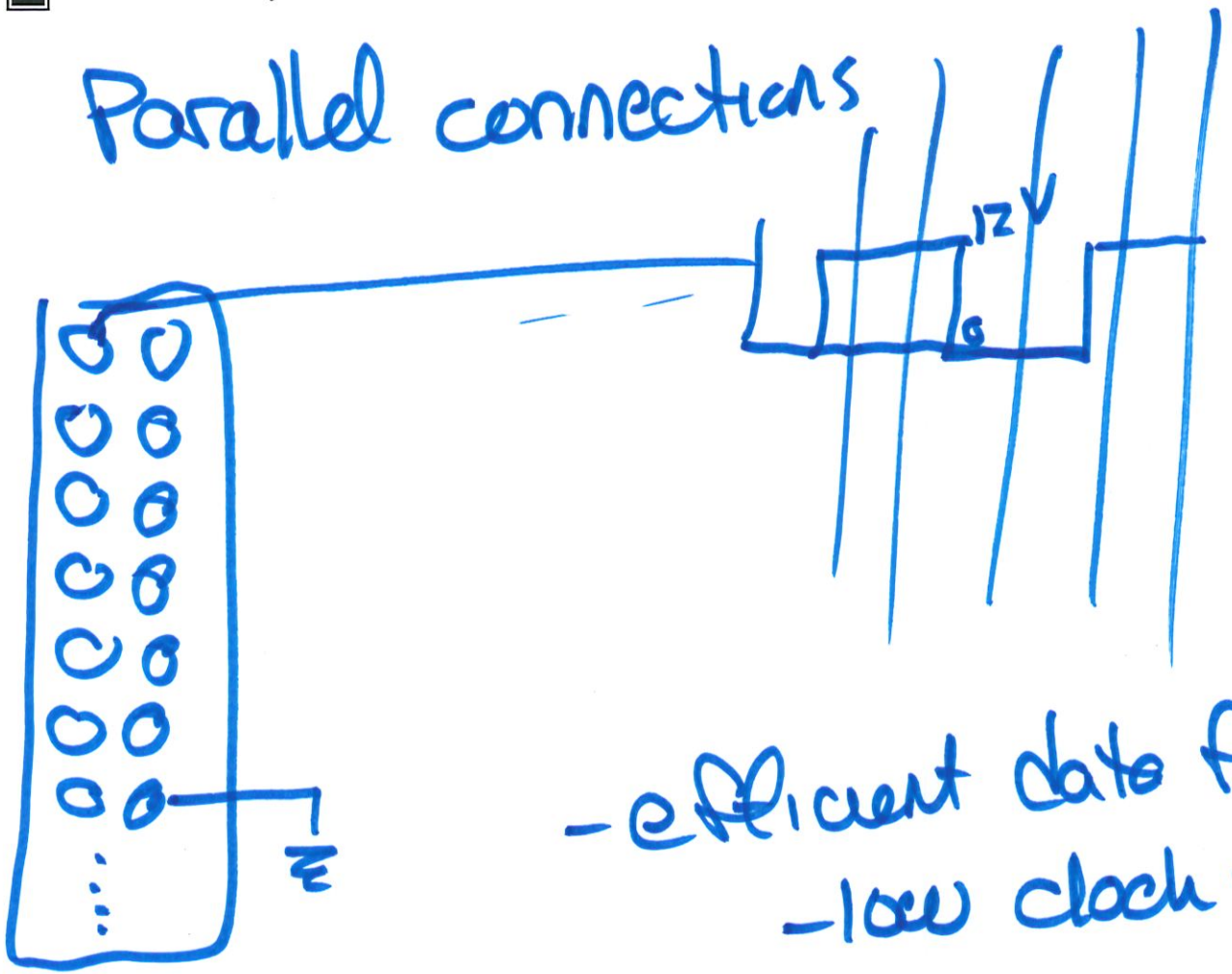
→ on/off → logic level levels

→ undirected & directed media

↑

fiber, copper wires

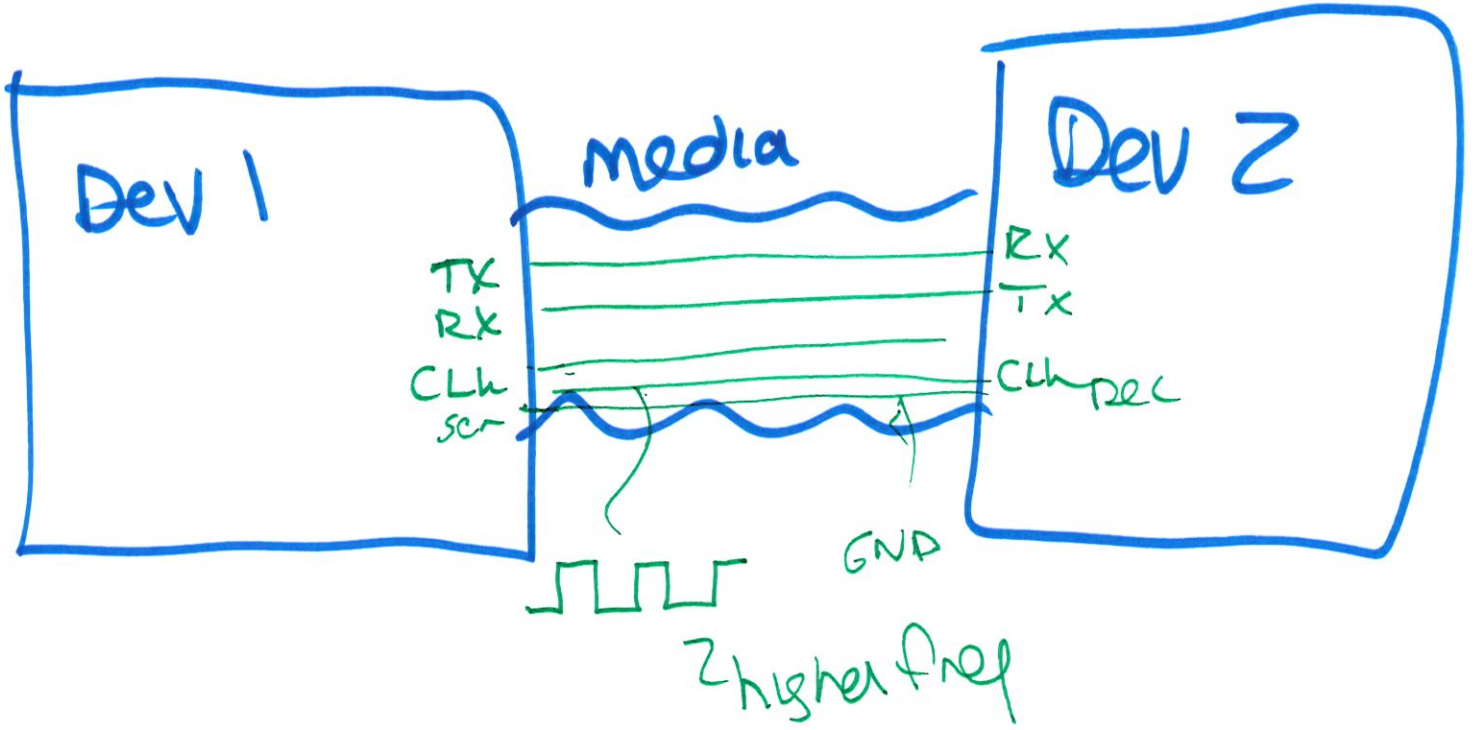
Parallel connections



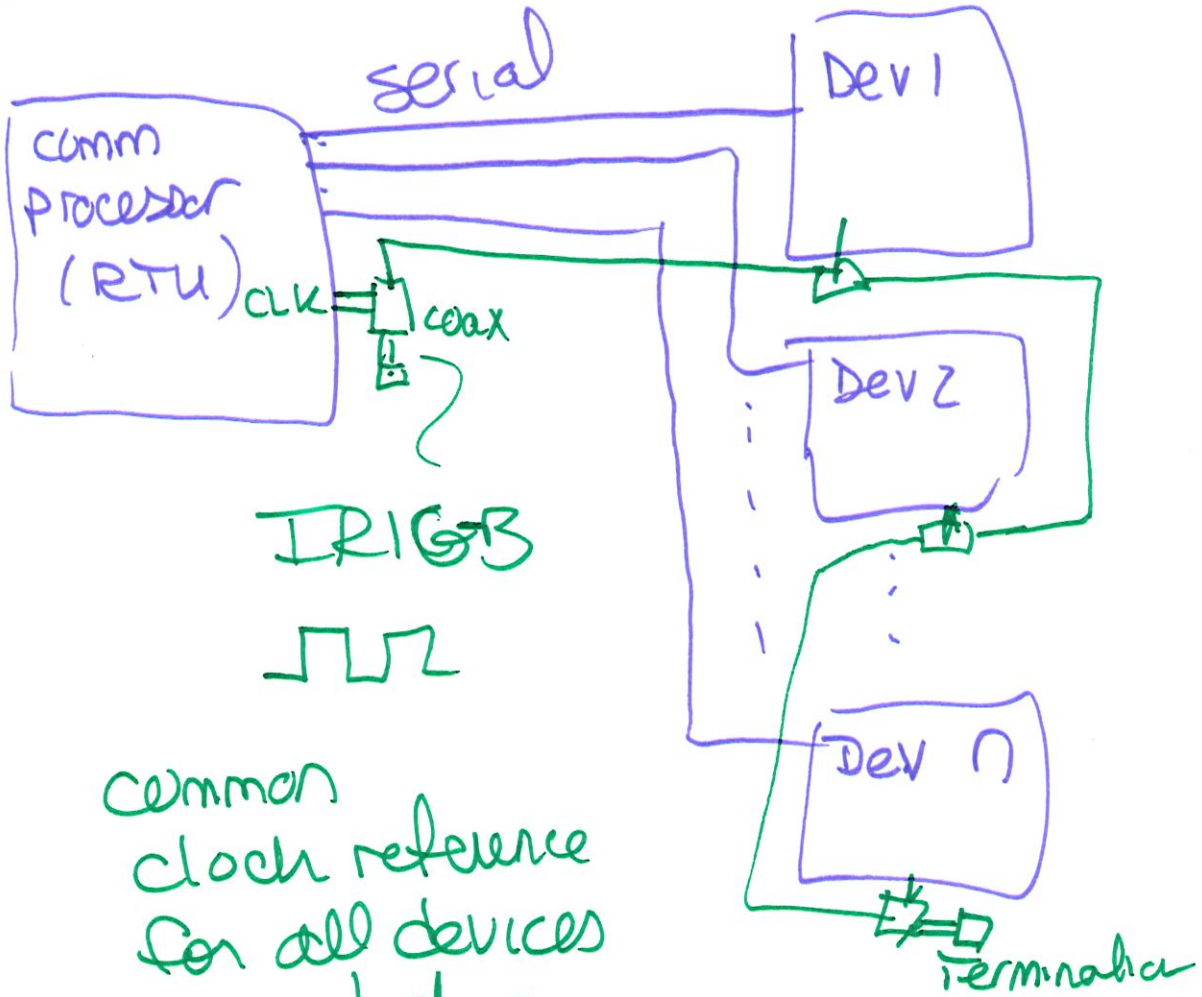
- efficient data flow
- low clock frequencies
- length limits

Data Synchronization

→ synchronous data transfer with a clock signal



External common clock reference



common clock reference for all devices in station

satellite clock systems

→ GPS (Global positioning system)

→ also transmit accurate clock reference

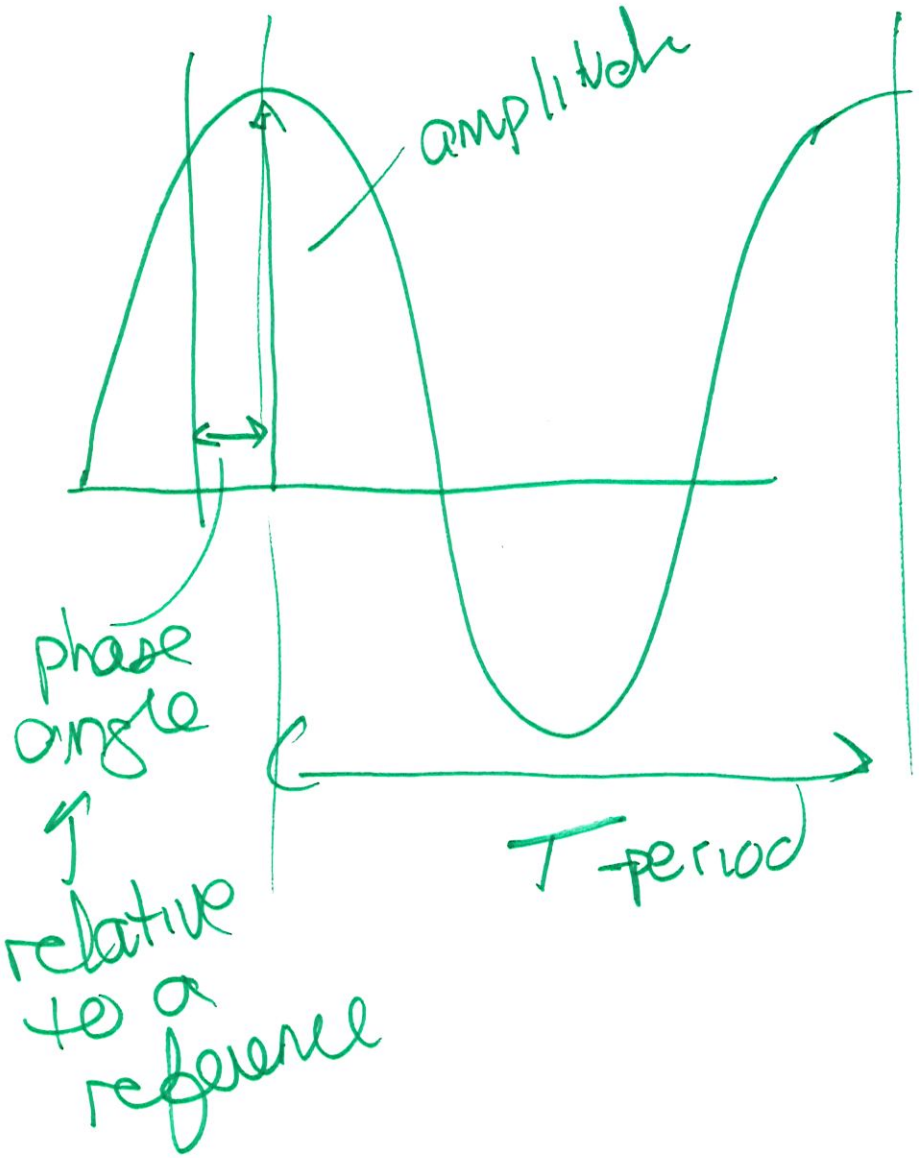
→ station → GPS antenna

↳ GPS clock

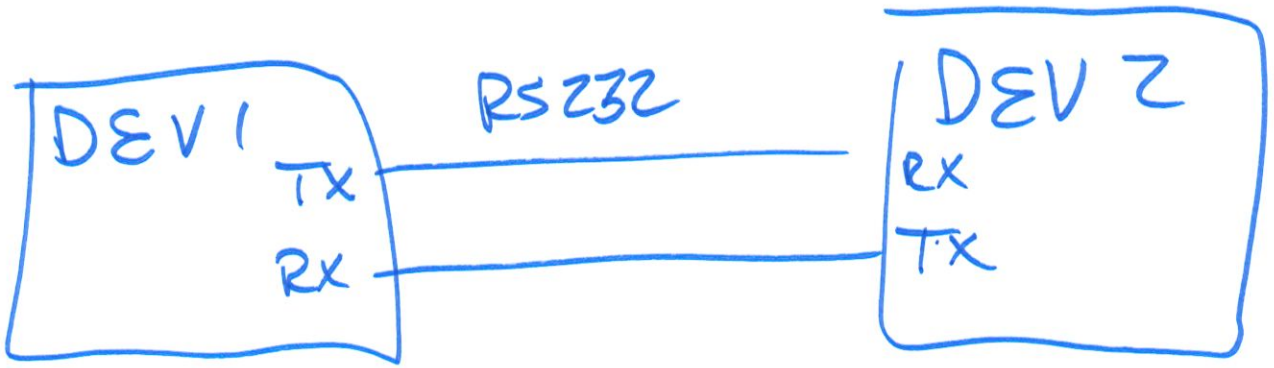
- captures the clock signal

- Clock distributes reference to devices in station → IRIG-B

— Ethernet protocols

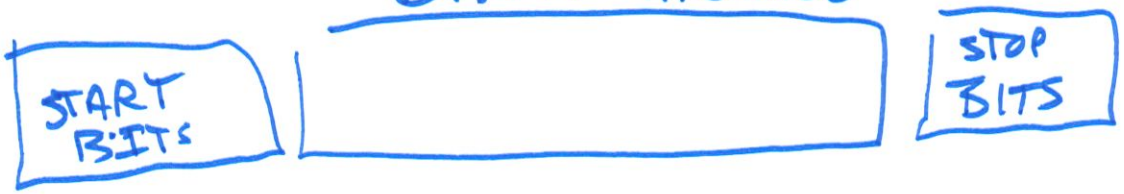

amplitude
phase angle
relative to a reference
T period

Asynchronous data transfer



No extra conductor for clock

DATA PACKAGE



Agreed number (configuration)

 → indicates data package coming
- sets clock frequency (capture by receiver)

- How do you identify if there are data errors?

① → Add parity bits

START		0110 1110 0110 1110	STOP
	parity bit(s)	DATA PACKET	

→ even → parity here is 0

or

odd parity → parity bit is 1

(2) Check sum

→ add the number of 1s in payload

→ send that number (binary number)

– in the example – send Bin equiv to 10

---

(3) cyclic redundancy check (CRC)

→ ~~PCRC~~ perform mathematical calculation using data

→ 16 or 32 CRC

→ Receiver can reproduce or correct data