

ECE 526

PROTECTION OF  
POWER SYSTEMS II

SESSION no. 10

## Failure modes (loss of comm)

POT: → depending on fault location + R<sub>F</sub>

- If one end sees fault in Zone 2 not zone 1
- Trip on Zone 2 time only or after other trips...

See zone 2 to  
know if power  
out - trip  
out

DCB: Fault inside line - Zone 2 picks up

- no block - high speed trip

Fault in Zone 2, outside line

→ High speed trip

after  
channel  
delays time

More delay than  
less  
over trip

DCUB - Tries to combine  
best features of both

- Loss comb  $\Rightarrow$  Loss of Guard  
 $\rightarrow$  still some risk of over

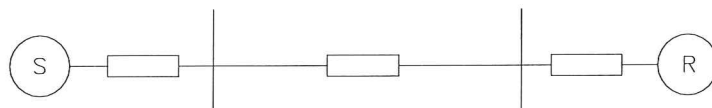
fitting

Goal for all 4

DUTT  
POTT  
DCB  
DCUB



- high speed tripping for faults anywhere in line between Bus S & Bus R
- with fault resistance

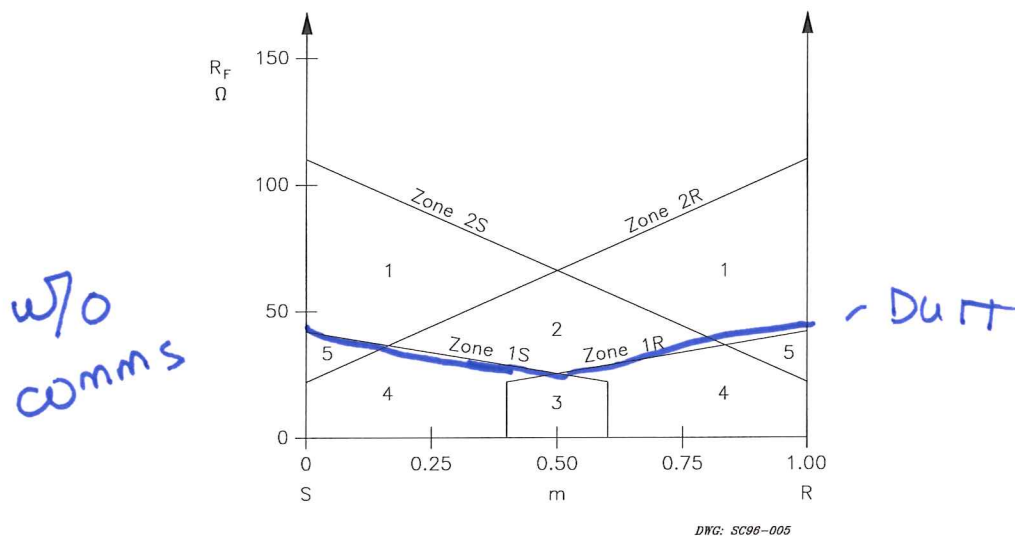


$$\begin{array}{lll} Z1S = 2\Omega \angle 90^\circ & Z1L = 8\Omega \angle 90^\circ & Z1R = 2\Omega \angle 90^\circ \\ Z0S = 6\Omega \angle 90^\circ & Z0L = 24\Omega \angle 90^\circ & Z0R = 6\Omega \angle 90^\circ \end{array}$$

DWG: SC96-004

Figure 4: Long Line Example System

Zone 2 Ground Directional Overcurrent Pickup: 0.5 A  
 Zone 1 Reactance Reach: 4.8  $\Omega$  (60%)  
 Zone 1 Resistive Reach: 50  $\Omega$



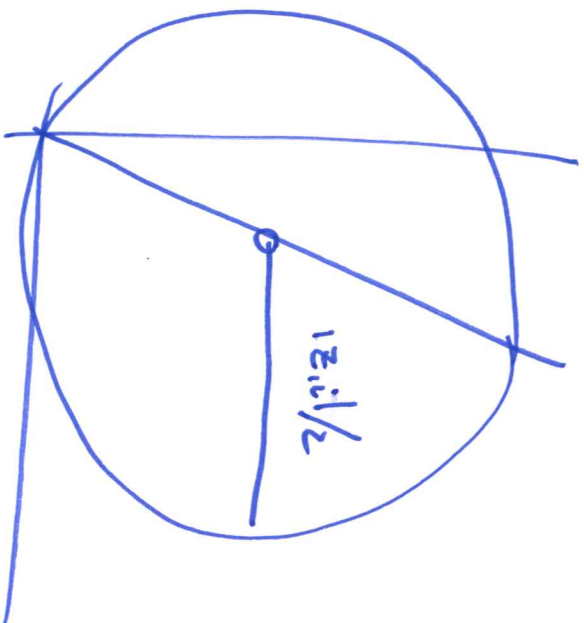
DWG: SC96-005

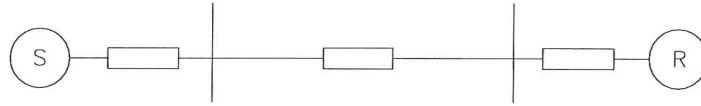
Figure 5: Long Line Resistive Fault Coverage Regions

Table 3: Long Line Coverage Regions

Region 1	37.4 $\Omega$
Region 2	13.7 $\Omega$
Region 3	4.7 $\Omega$
Region 4	25.6 $\Omega$
Region 5	6.6 $\Omega$
<b>Total</b>	<b>88.0 <math>\Omega</math></b>

Table 3 lists the area, in ohms, of each region for the long line system. Later, we will see that each protection scheme clears faults in differing times for the various regions. The unit of area measure for these regions is ohms to simplify the comparisons between the long and short lines. To determine the area of each region, we calculated the geometric area in ohms (vertically) times m per unit of the line (horizontally).



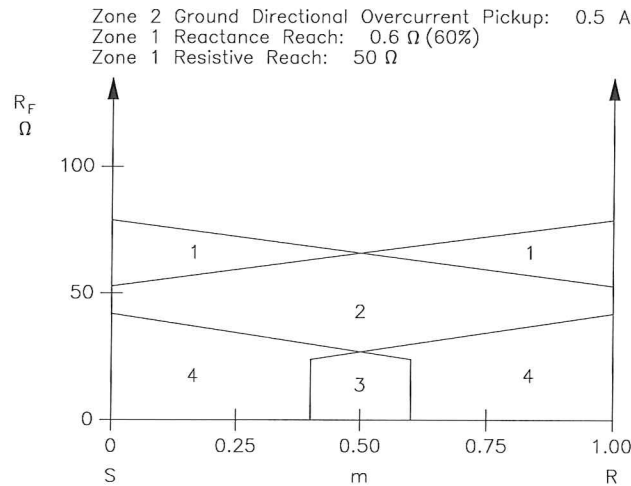


$$\begin{array}{lll} Z1S = 2 \Omega \angle 90^\circ & Z1L = 1 \Omega \angle 90^\circ & Z1R = 2 \Omega \angle 90^\circ \\ Z0S = 6 \Omega \angle 90^\circ & Z0L = 3 \Omega \angle 90^\circ & Z0R = 6 \Omega \angle 90^\circ \end{array}$$

DWG: SC96-006

Figure 6: Short Line Example System

mho



DWG: SC96-007

Figure 7: Short Line Resistive Fault Coverage Regions

Table 4: Short Line Coverage Regions

Region 1	13.0 $\Omega$
Region 2	32.0 $\Omega$
Region 3	9.8 $\Omega$
Region 4	17.7 $\Omega$
<b>Total</b>	<b>72.5 <math>\Omega</math></b>

In all cases, we assumed the additional parameters shown in Table 5.

Table 5: Additional System Parameters

Element Operating Time	1.0–1.5 cycles
Breaker Clearing Time	2.0 cycles
Channel Operate Delay	1.0 cycle
Zone 2 Time Delay	20 cycles



51/2  
7/15  
017

### Direct Underreaching Transfer Trip (DUTT)

Figure 9 shows the fault clearing time areas for DUTT protection. Faults detected by both Zone 1 elements are cleared without time delay at both ends. Faults detected by a single Zone 1 element are cleared with an additional 1-cycle time delay to account for the communication channel delay. In-section Zone 2 faults are cleared simultaneously in 25 cycles, or sequentially in 50 cycles, depending on their location and resistance.

For the long line case, the DUTT figure of merit is calculated:

$$\rho_{TR} = \frac{\left(\frac{50 \text{ cyc} \cdot 37.4 \Omega}{88 \Omega}\right) + \left(\frac{25 \text{ cyc} \cdot 13.7 \Omega}{88 \Omega}\right) + \left(\frac{4.5 \text{ cyc} \cdot (25.6 \Omega + 6.6 \Omega)}{88 \Omega}\right) + \left(\frac{3.5 \text{ cyc} \cdot 4.7 \Omega}{88 \Omega}\right)}{88 \Omega} = 307 \times 10^{-3} \quad \text{Equation 3}$$

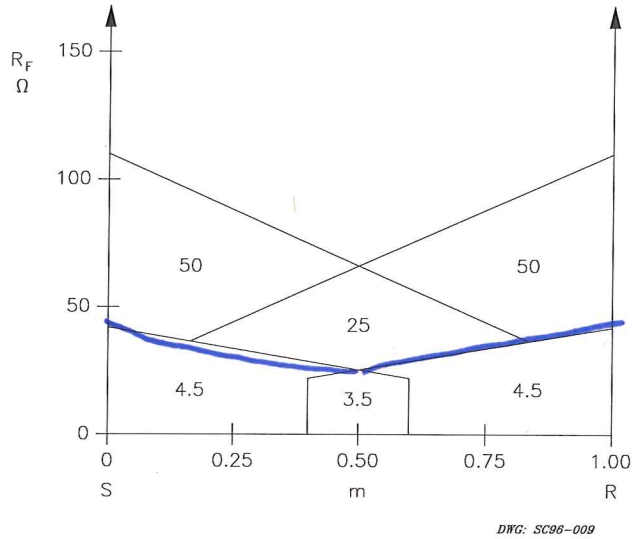


Figure 9: Fault Clearing Times for DUTT Protection, Long Line

### Permissive Underreaching Transfer Trip (PUTT)

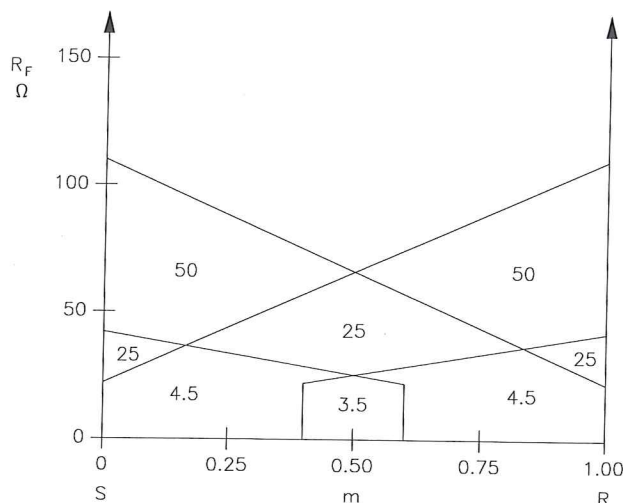
Figure 10 shows the PUTT fault clearing times. Resistive faults are cleared quickly by the PUTT scheme only if they are detected by both Zone 1 elements, or by the local Zone 1 and remote Zone 2 elements. Faults that fall into the area covered by both Zone 2 elements are cleared in 25 cycles, and faults that fall into a single Zone 2 are cleared sequentially in 25 or 50 cycles.

For the long line case, the PUTT figure of merit is:

$$\rho_{TR} = \frac{\left(\frac{50 \text{ cyc} \cdot 37.4 \Omega}{88 \Omega}\right) + \left(\frac{25 \text{ cyc} \cdot (13.7 \Omega + 6.6 \Omega)}{88 \Omega}\right) + \left(\frac{4.5 \text{ cyc} \cdot 25.6 \Omega}{88 \Omega}\right) + \left(\frac{3.5 \text{ cyc} \cdot 4.7 \Omega}{88 \Omega}\right)}{88 \Omega} = 324 \times 10^{-3} \quad \text{Equation 4}$$



410 8/15



DWG: SC98-010

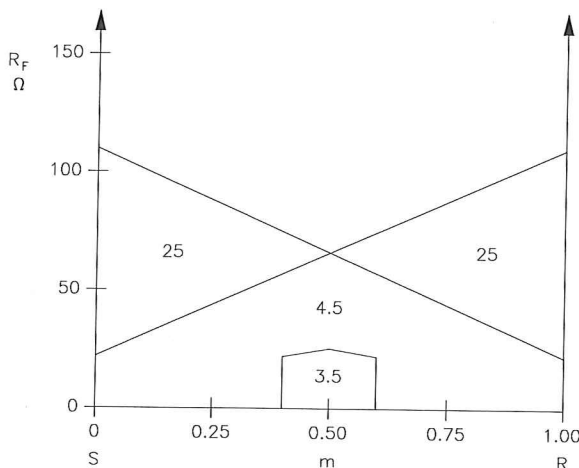
Figure 10: Fault Clearing Times (cycles) for PUTT Protection, Long Line

### Permissive Overreaching Transfer Trip (POTT)

Figure 11 shows the POTT fault clearing times. Resistive faults are cleared in communication-aided time if they are detected by both Zones 2 elements. Faults that fall into a single Zone 2 are cleared sequentially in 25 cycles, assuming the local relay Zone 2 dropout time is equal to or longer than the remote relay Zone 2 pickup time.

For the long line case, the POTT figure of merit is:

$$\rho_{TR} = \frac{\left( \frac{25 \text{ cyc} \cdot (37.4 \Omega + 6.6 \Omega)}{88 \Omega} \right) + \left( \frac{4.5 \text{ cyc} \cdot (13.7 \Omega + 25.6 \Omega)}{88 \Omega} \right) + \left( \frac{3.5 \text{ cyc} \cdot 4.7 \Omega}{88 \Omega} \right)}{88 \Omega} = 167 \times 10^{-3} \quad \text{Equation 5}$$

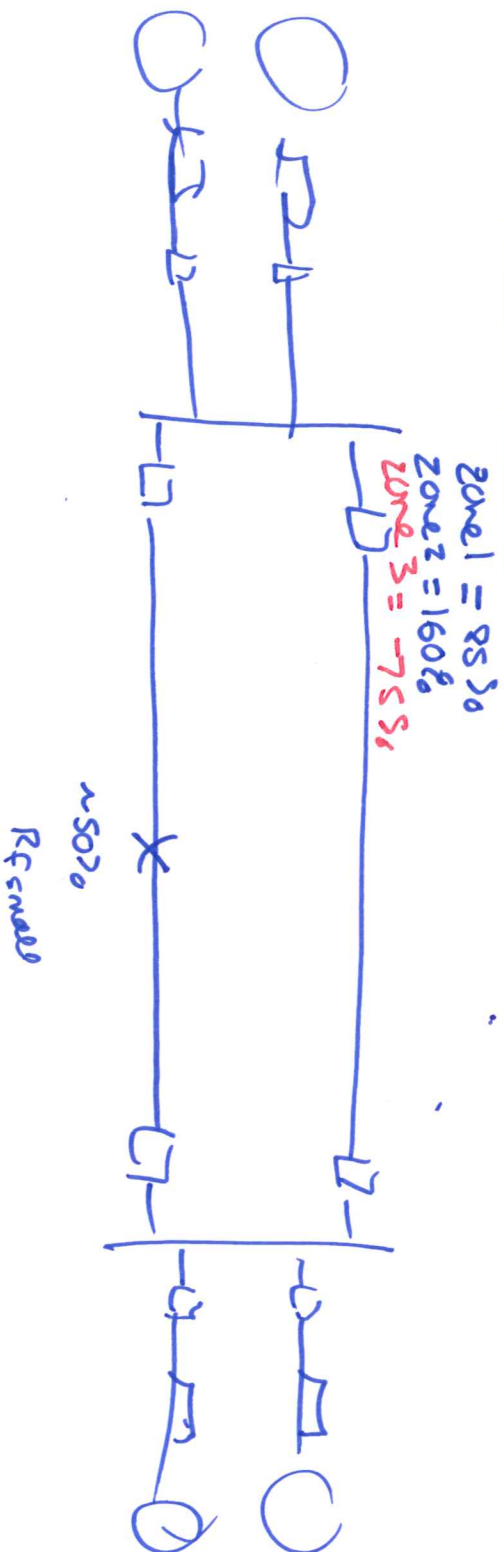


DWG: SC98-011

Figure 11: Fault Clearing Times (cycles) for POTT Protection, Long Line

### Directional Comparison Blocking (DCB)

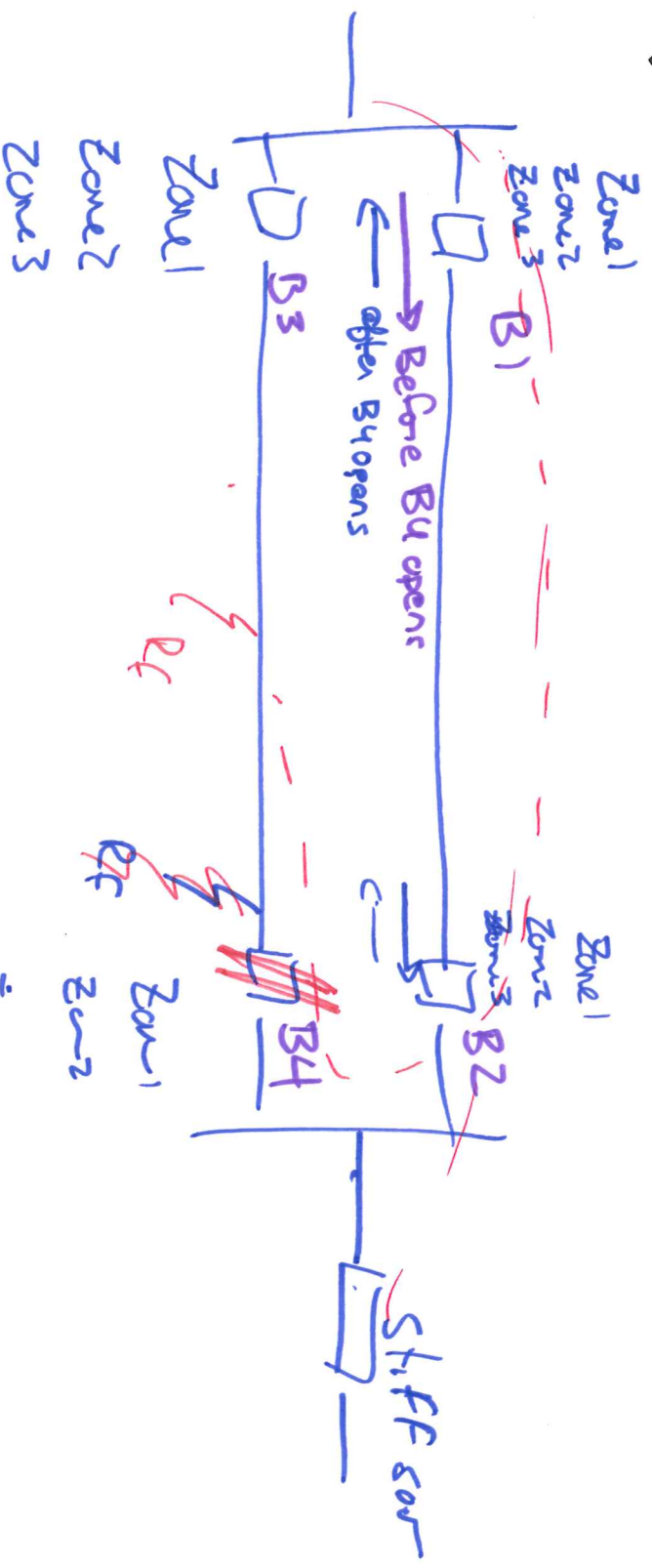
Figure 12 shows the DCB fault clearing times. Both ends operate and clear in 5 cycles when the fault resistance is low enough for both Zone 2 elements to operate. This is very similar to the POTT scheme. The 5-cycle time

Other challenges1. Parallel lines

→ would trip both lines ....

— add reverse looking Zone 3 for each - over each zone 2 ---

→ Zone 3 to 7550



Current reversed for relay at B1 & B2

B2 → Zone 3 deasserts

Zone 2 asserts, already received  
Zone 2 from B1  
(comm delays)

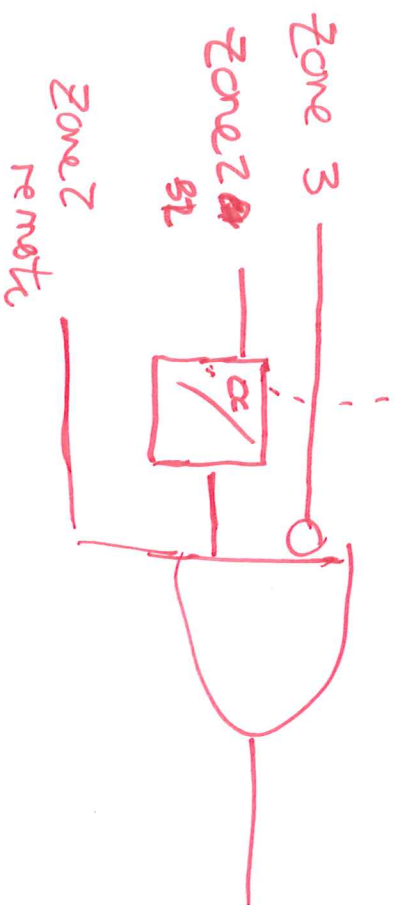
B2 trips

B1. Zone 2 deserts

Zone 3 picks up

Current revealal time in addition  
to zone 3

several cycles



# Power electronic generator

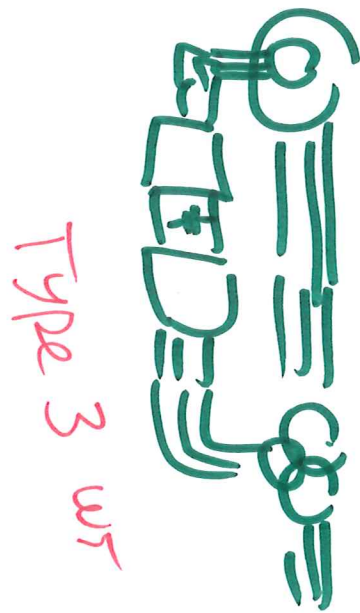
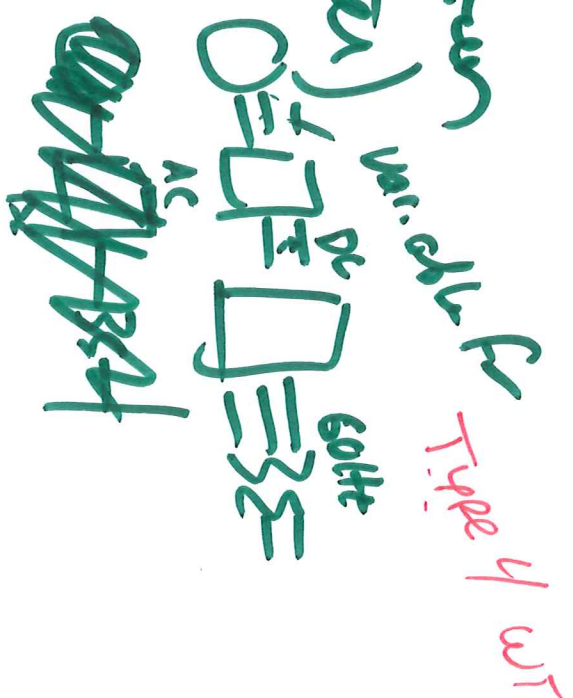
(con VSC HVDC converter)



voltage source converter

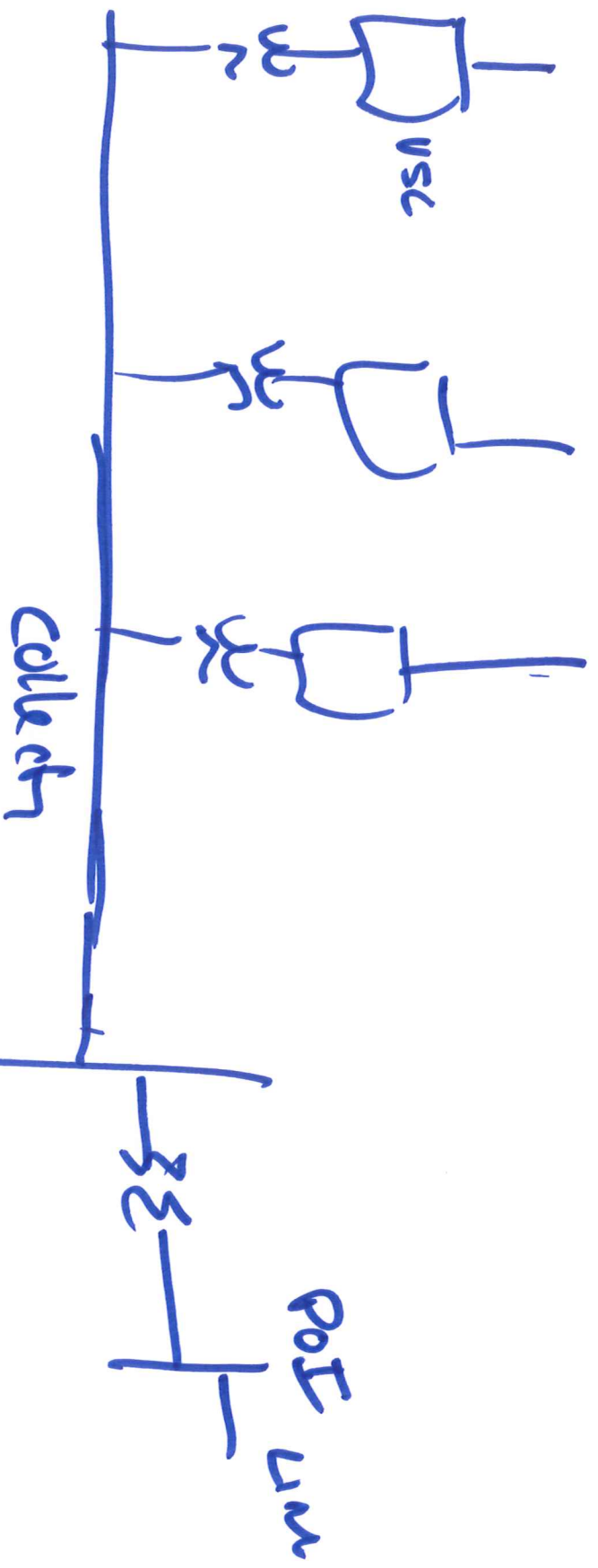
- ① - limit current to 110% - 120% of rated

- ② - unity pf most of time
- ③ - IFC low voltage condition provide Q



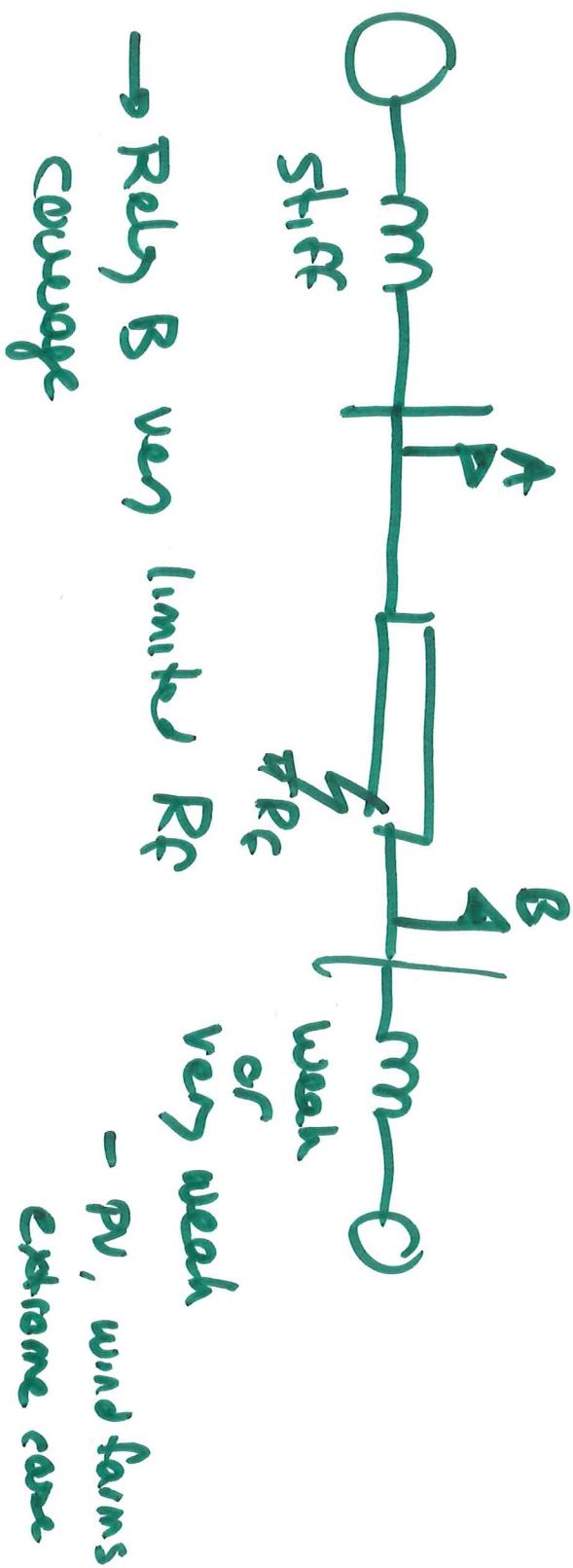
Type 3 WT





4. Not all are always ~~on~~ online  
- further limit

# Weak in feed at one end - POT or DCUB



- Relay A sees fault in Zone 2
- Relay B doesn't see fault in Zone 2, at least until A opens



- Options (alternative schemes)

1. Line current different
2. DCB
3. Echo keying scheme
  - Starts to look more like direct transfer trip

Variation

