Static VAr Compensator

- Shunt/parallel connected TCR
  - Three phase Y or Δ connection
  - 6 or 12 pulse connection
- Connected in parallel with:
  - Harmonic filters (capacitive at fundamental freq)
  - Fixed capacitor banks
  - or Thyristor switched capacitor modules
- Firing synchronization based on voltage

Circuit Configuration

- Fixed capacitor
- 12 pulse config,
- More than one harmonic filter
  - 11th, 13th, high pass for 12 pulse
  - 5th, 7th also needed for 6 pulse
SVC Circuit Configuration with TSC

- Thyristor switched capacitor

TSC On/Off

TCR Internal Control

B_{ref} or I_{ref}

Firing Pulses

TCR TSC1 TSC2 TSC3 Harmonic Filters

TSC Gate Pulse Generators

Firing Pulses

Synchronization

TSC Power Circuit

- Trapped charge
- Transient free switching requires switching when $V_{\text{switch}}=0$
- If voltage drops when capacitor out of circuit: can’t reach $V_{\text{cap}}$

Synchronization
TSC Power Circuit

- Integral cycle control
- Switch based on:
  - \( V_{\text{switch}} = 0 \) and Command
  - or
  - \( \text{Switch} = \text{min} \) and Command
- Output sent to gate pulse generator
- Continuous pulse

TSC Controls
Test System

- TSC model tested in simple system.
- Stiff source behind a transformer
- Refer to distribution voltage level
- Single TSC in parallel with lagging power factor load
- Simulated using ATP
- Per phase equivalent first

Case 1: No line inductance

- Capacitor on-off command varied every 6 cycles
- Note that switch voltage has offset
- Voltage difference reaches zero while not conducting (sinusoidal part of waveform)
- Integral cycle current waveforms
Case 1: No line inductance

Synchronization

Thyristor Currents

(file tsc1.pl4; x-var t) c:SW2 -VLO c:SW1 -CAPLO
Case 2: Line inductance

- Capacitor on-off command varied every 6 cycles
- Again note that switch voltage has offset
- Voltage difference doesn’t reach zero while not conducting
Case 2: With Line inductance

Bus Voltage

(file tsc2.pl4; x-var t) v:CAPHi -