COE/EE 243
Homework Assignment #6
Due Tuesday March 25 by 2:00pm

Show your work on all of the problems below. If you want to see sample problems with solutions go to `http://web.ddpp.com/student/student.html` or the examples on the course web page.

1. Realize the following functions using a PLA (try to optimize use of the PLA):

$$\begin{aligned} X &= ABD + A'C' + BC + C'D' \\ Y &= A'C' + AD + C'D' \\ Z &= CD + A'C' + AD + AB'D \end{aligned}$$

   Provide the PLA table and sketch the equivalent circuit. How many gates and gate inputs are needed?

2. Repeat problem 1 using the PAL shown on the next page. Fill in the appropriate connections.

   How many gates and gate inputs are needed. Does this differ from the number required with the PLA? Explain.

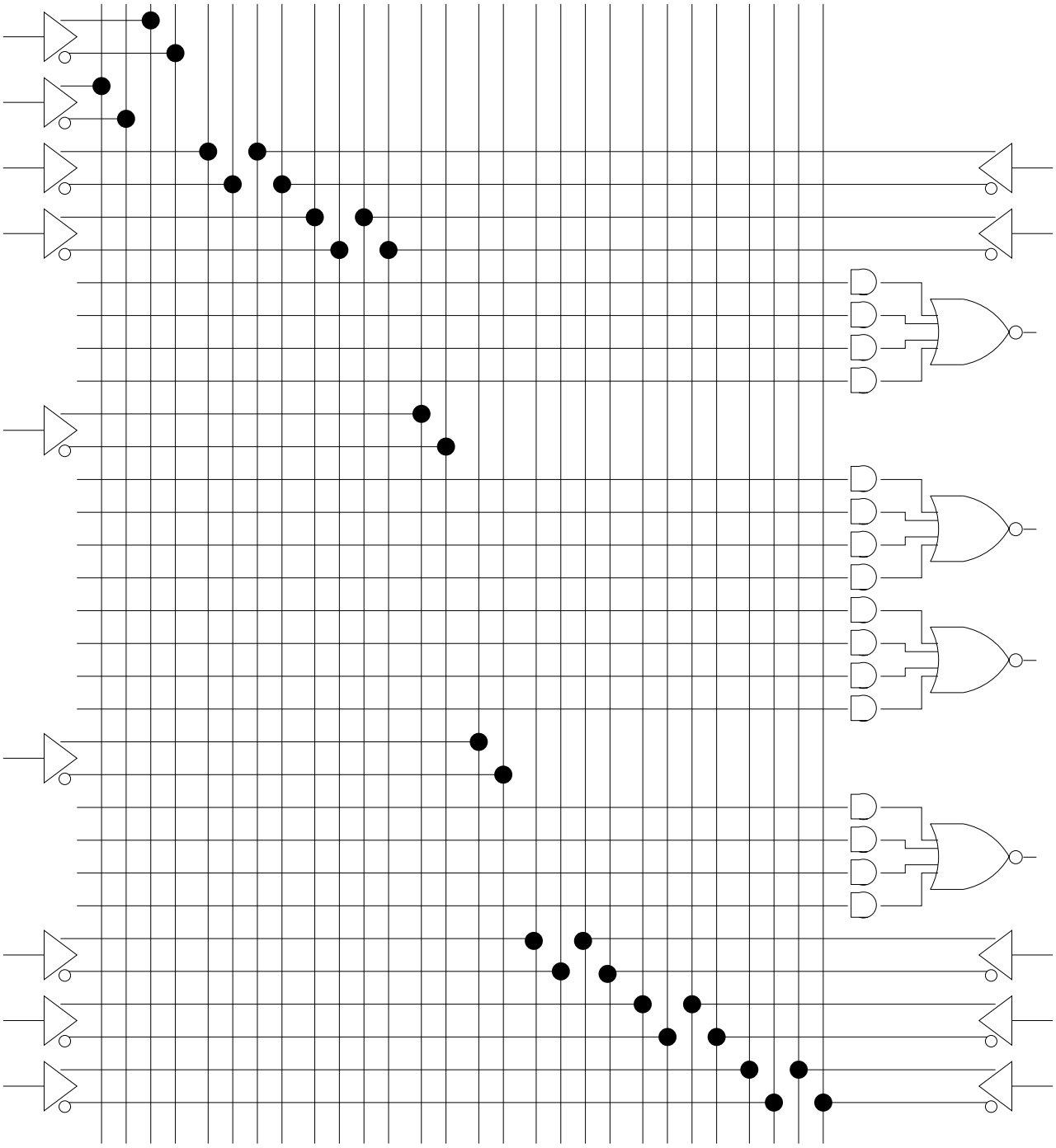
3. Design a full adder module with data input X and Y, carry input C_{in}, Sum output S, and Carry output C_{out} using:

   (a) A 3-8 decoder and NAND gates

   (b) 4-to-1 multiplexers

4. Problem 5.28 in your text

5. Design a BCD adder that adds two BCD digits and produces a BCD result and a carry output and indicates an overflow.



PAL 14L4