COE/EE 243 Homework Assignment #7 Due /Friday April 11 by 5:00pm

Show your work on all of the problems below. If you want to see sample problems with solutions go to http://www.ddpp.com/student/student.html or the examples on the course web page.

- 1. Add extra logic gates to a clocked D flip-flop to create a clocked JK flip-flop.
- 2. Problem 7.4 of your text
- 3. Problem 7.5 of your text
- 4. Derive the state equation for a SR latch (based on NOR gates). Next modify the latch such that S=R=1 will set the latch. In addition, S=0, R=1 will reset, S=1, R=0 will set the latch and S=R=0 will hold the present state.
- 5. Complete the timing diagram for a clocked master-slave flip-flop receiving the following input waveform sequence. Designate P as the output of the first flip-flop, and Q as the output of the master-slave combination.



Use propogation delay of 0.

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6. Complete the timing diagram for a clocked master-slave flip-flop receiving the following input waveform sequence. Designate P as the output of the first flip-flop, and Q as the output of the master-slave combination.

Use propogation delay of 0.



- 7. Problem 7.2 in your text
- 8. Problem 7.3 of your text
- 9. Repeat problem 7.2 in your text if the S input is now the D input to a D latch configured like the one in Figure 7-12 and the R input is the Control input.