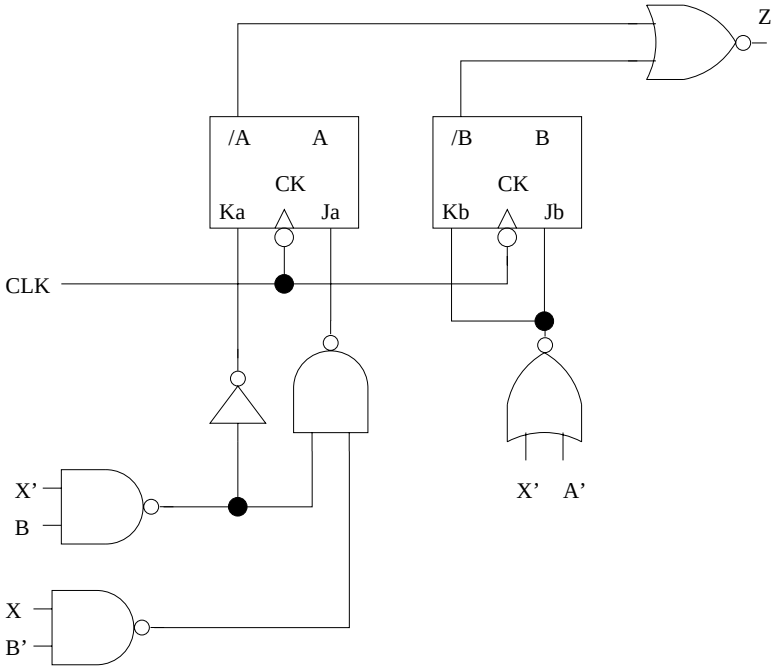
EE/CompE 243
State Machine Analysis Examples

1. For the state machine shown in the figure below do the following:

(a) Find the excitation equations for the flip-flops. Then construct a transition table, a state table, and a state diagram. Is this a Moore Machine or a Mealy Machine?

(b) What is the output sequence when the input sequence is X=01100?

(c) Draw a timing diagram for the input sequence from part (b). Show P_c, X, A, B and Z. Assume input changes between clock pulses.



(a) Derive state equations

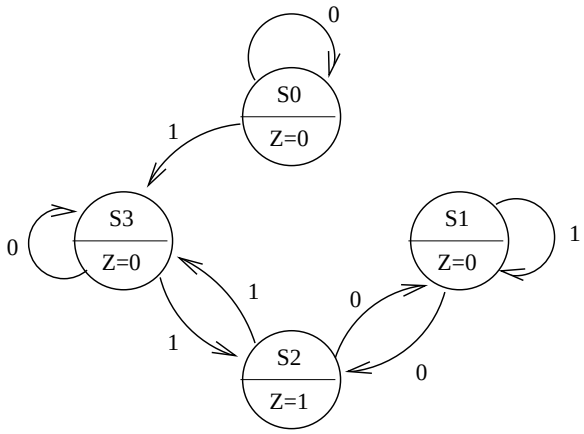
$$\begin{aligned} J_A = ((X'B)'(XB')')' &= X'B + XB' \\ K_A &= X'B \\ J_B = (X' + A')' &= XA \\ K_B = (X' + A')' &= XA \\ A+ = J_A Q' + K_A' Q &= (X'B + XB')A' + (X'B)'A \\ &= A'BX' + A'B'X + AX + AB' \\ B+ = J_B Q' + K_B' Q &= XAB' + (XA)'B \end{aligned}$$

$$= AB'X + BX' + A'B$$
$$Z = (A' + B')' = AB$$

It is a Moore machine, since Z only depends on A, B not on X

Present State AB	Next State (A+B+) X=0	X = 1	Z
00	00	10	0
01	11	01	0
11	01	10	1
10	10	11	0

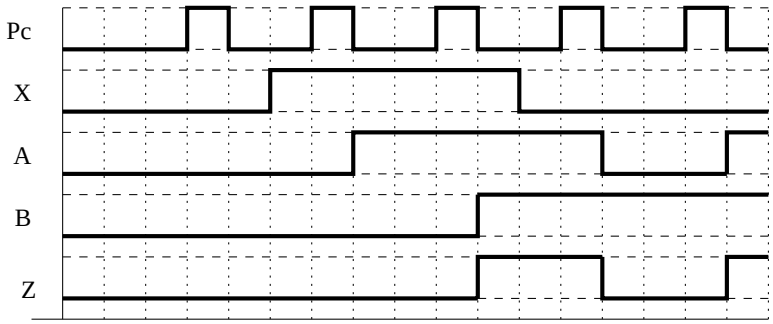
Present State AB	Next State (A+B+) X=0	X = 1	Z
S0	S0	S3	0
S1	S2	S1	0
S2	S1	S3	1
S3	S3	S2	0



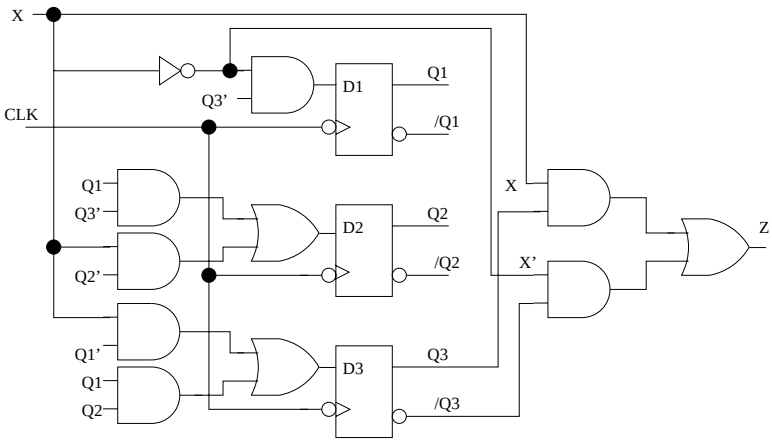
(b) Based on the state/output diagram above, we see that Z will be 1 only when $AB = 11$. Note also that we can consider the initial output for Z to be a false output until the first falling edge of the clock. So we get $Z = (0)00101$ as shown in the figure below.

(c) Timing diagram for network:

Propagation delay is assumed to be 0.

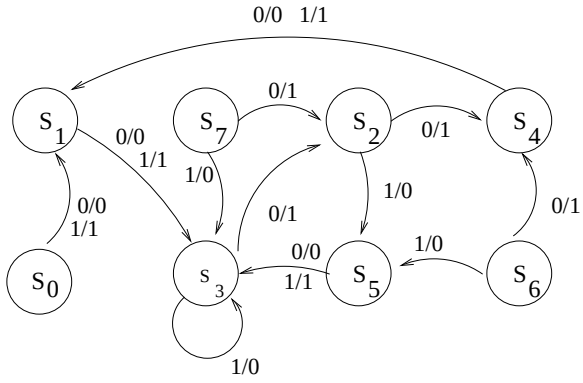


2. Do the following for the state machine shown below:

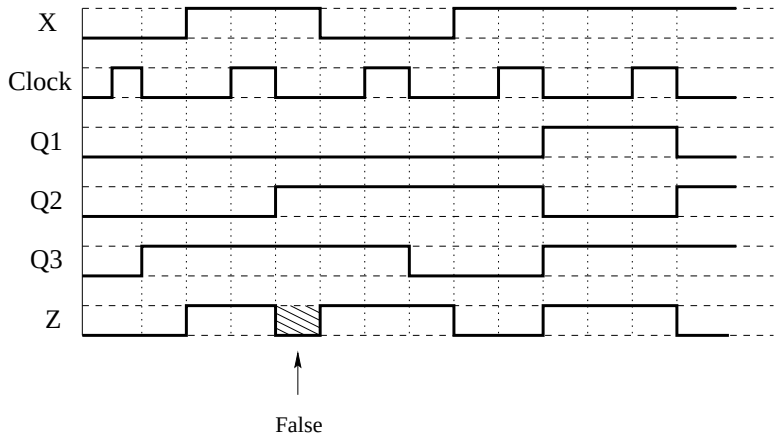


a. Construct a state table and state diagram

state	$Q_1Q_2Q_3$	$Q_1+Q_2+Q_3+$ X=0	$Q_1+Q_2+Q_3+$ X=1	Z X=0	Z X=1
S_0	000	001	001	0	1
S_1	001	011	011	0	1
S_2	010	100	101	1	0
S_3	011	010	011	1	0
S_4	100	001	001	0	1
S_5	101	011	011	0	1
S_6	110	100	101	1	0
S_7	111	010	011	1	0



b. Draw a timing diagram for the network. Show X, clock, Q1, Q2, and Q3. Use the input sequence X=01011 and assume that X changes midway between clock pulses. Indicate any false output changes.

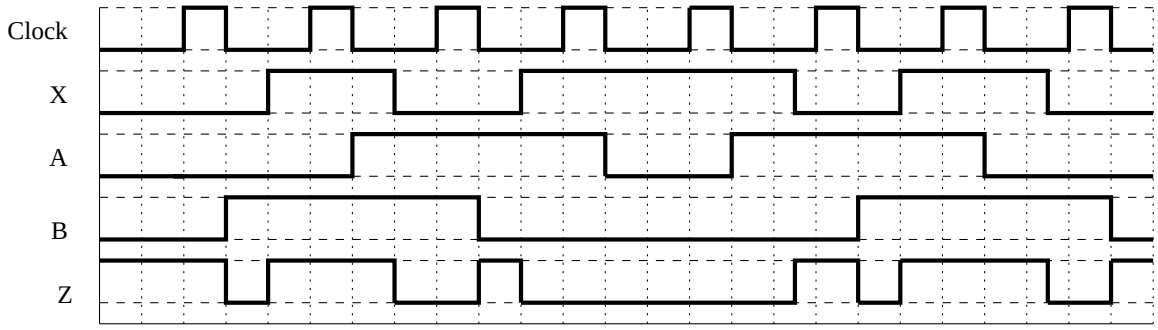


c. Compare output sequence from timing diagram with the one predicted by the state diagram.
From timing diagram: 0 1 (0) 1 0 1
From state diagram: 0 1 1 0 1

d. How can you correct the difference?
By changing input on falling edge of the clock the false outputs can be eliminated.

3. A Mealy synchronous state machine has 1 input, 1 output and 2 flip-flops. A timing diagram is shown below. Construct a state table and a state diagram

Propagation delay is assumed to be 0 division



Since the timing diagram shown here is for a Mealy sequential network, we know that the Mealy network depends on both the present state and the inputs.
For this network X is the input and Z is the output and Q_1, Q_2 represent the present states.

The state table can be constructed by simply finding the output value(Z) for various input combinations from the timing diagram.

Present State	Next State (Q_1+Q_2+)		Z_1Z_2	
Q_1Q_2	X=0	X=1	X=0	X=1
00	01	10	1	0
01	00	11	0	1
10	11	00	1	0
11	10	01	0	1

Present State	Next State (Q_1+Q_2+)		Z_1Z_2	
Q_1Q_2	X=0	X=1	X=0	X=1
S0	S1	S2	1	0
S1	S0	S3	0	1
S2	S3	S0	1	0
S3	S2	S1	0	1