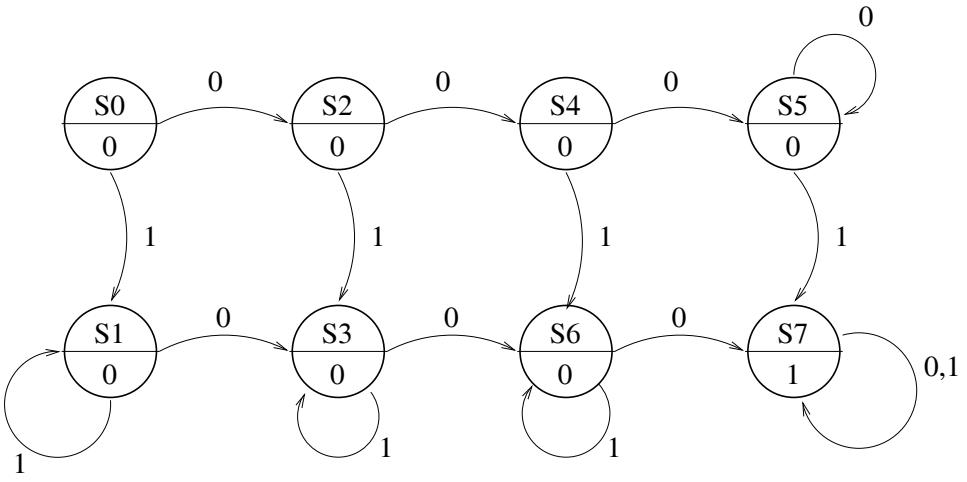
EE/CompE 243
Additional State Machine Design Examples

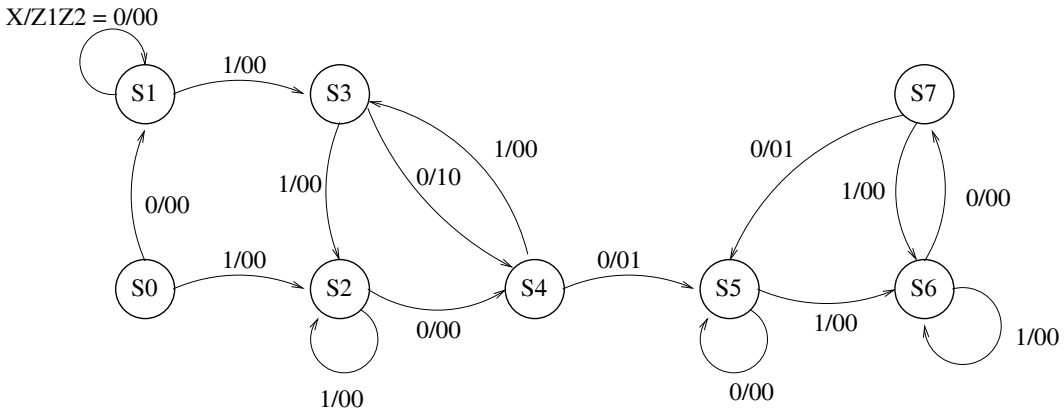
1. Design a Moore machine state diagram for a sequence detector that outputs a 1 after receiving a sequence with at least one 1 and three 0's in any order.

Present State	Input Sequence	Next State X=0	Next State X=1	Output Z
S0	Init.	S2	S1	0
S1	1	S3	S1	0
S2	0	S4	S3	0
S3	01	S6	S3	0
S4	00	S5	S6	0
S5	000	S5	S7	0
S6	001	S7	S6	0
S7	0001	S7	S7	1



2. Design a Mealy machine state table for a sequence detector with one input X and two outputs (Z_1 and Z_2). Output $Z_1 = 1$ after a sequence 010 if a 100 hasn't been received already, in which case $Z_1 = 0$. Output $Z_2 = 1$ after 100 has been received.

Present State	Input Sequence	Next State X=0	Next State X=1	Z_1 Z_2 X=0	Z_1 Z_2 X=1
S0	Init.	S1	S2	00	00
S1	0	S1	S3	00	00
S2	1	S4	S2	00	00
S3	01	S4	S2	10	00
S4	10	S5	S3	01	00
S5	100	S5	S6	00	00
S6	1	S7	S6	00	00
S7	10	S5	S6	01	00



3. Design a Moore network state diagram for a state machine with one input and one output. A sequence of 101 toggles the output between 0 and 1. Note that the sample sequence changes the output *after* the 101, not at the same time as the last 1. Can start in either S0 or S1.

Example:

X=	0	1	0	1	0	1	0	0	1	0	1	0	1	1	0	1	0	x	
Z=	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	1	1	

Present State	Input/Ouput Sequence	Next State X=0	Next State X=1	Output Z
S0	0/0	S0	S1	0
S1	1/0	S2	S1	0
S2	10/0	S0	S3	0
S3	101/0	S5	S4	0
S4	1/1	S5	S4	1
S5	10/1	S6	S7	1
S6	0/1	S6	S4	1
S7	101/1	S2	S1	1