Final Exam Topics

Chapter 2:
- Number systems (decimal, hexadecimal, octal, binary)
- Converting between different bases
- Binary arithmetic–add, subtract, multiply
- 2’s and 1’s compliment math
- Binary codes

Chapter 3:
- Understanding differences between logic families
- Voltage levels versus logic levels
- Fan out
- Propagation delay
- Problems with noise
- Noise margin
- Anything in this chapter will be covered only in short answer questions to see if terms understood

Chapter 4:
- Basic boolean operators
- Logic symbols
- truth tables
- logic diagrams
- Multiplying out/factoring expressions
- Sum of products
- Product of sums
- Applying theorems and axioms
- Inversion
- Duality
- XOR/XNOR
- Using truth tables in network design
- Minterm expansions SUM(m(1,3,5,...))=terms with f=1
- Maxterm expansions PROD(M(1,3,5,...))=terms with f=0
- Don’t cares (incomplete specification)
- Karnaugh maps (3,4,5 Var)
- Quine-McCluskey
• You will be asked to simplify expressions, get standard POS or SOP from set of minterms etc.....

• Multilevel networks
  – count levels
  – number of gates
  – number of gate inputs

• Functionally complete sets

• NAND networks with 2 or more levels

• NOR networks with 2 or more levels
  – converting AND-OR networks to NAND or NOR only network
  – creating NAND or NOR network from expression

• Multiple output networks
  – using common terms to reduce number of gates and inputs

Chapter 5 :
• Multiplexers
  – 4 to 1, 8 to 1, etc
  – implement boolean functions with MUXs

• Decoders
  – 2 to 4, 3 to 8, 4 to 16, etc.
  – Combine outputs of decoder with logic gates to realize expressions

• Programmable Logic Arrays (PLA’s)
  – can use to realize functions
  – AND - OR network where can program connections for ANDs and ORs

• Programmable Array Logic (PAL’s)
  – can use to realize functions
  – AND - OR, AND-NOR, etc. network where can program connections for ANDs only.

Chapter 7 :
• Flip flops and latches
• Basic understanding
• Timing Diagrams
• Characteristic Equations
• Analysis of synchronous sequential networks
- Excitation equations for flip-flop inputs
- Substitute excitation equations into flip-flop characteristic eqs.
- Construct transition table with output values added
- Create state table
- Draw state diagram (optional)
- Moore versus Mealy networks
- False outputs
- Be able to start from timing diagram or state diagram
- Flip-flop state transition tables
- Implementing circuits using flip-flops
- Derivation of state graphs and tables for Mealy and Moore Networks from set of objectives
- Clocked Synchronous State-Machine Design Summary
- Design process is reverse of analysis process:
  1. Construct state/output table corresponding to word description. Can also start with a state diagram.
  2. Minimize number of states in table.
  3. Choose set of state variables.
  4. Create transition/output table.
  5. Choose flip-flop type.
  6. Create excitation table.
  7. Derive excitation and output equations.
  8. Draw the logic diagram.
  9. Verify the implementation
  10. Simulate
  11. Implement in hardware

Chapter 8:
- MSI circuits for sequential logic
- IC Shift Registers (74178)
- IC counters (74x163)
- 3 state buffers and 3 state bus
- Programmable Logic Devices for sequential circuits
- PALs–some have built-in flip-flops
- Output macrocells
Chapter 10:
- Field programmable gate arrays
- ROMs, PROMs, EPROMs, EEPROMs
  - essentially decoder combined with memory array
  - realize functions with ROM

Part of Chapter 5 and Chapter 8:
- Networks for addition and subtraction
- full adder circuits
- binary adders, accumulators
- Circuits for mult/division