# COE/EE 243: DIGITAL LOGIC
# Spring 2003

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**OFFICE HOURS:** M,W,F: 3:30-4:30pm
T, Th: 9:30-10:30am
Any time my door is open

**CLASS TIME:** EE/COE 243 MWF 10:30am, JEB Rm. 104
Other classes EE 422 MWF 12:30pm

**COURSE WEB PAGE** `http://www.ee.uidaho.edu/ee/digital/EE243/`

I will post summaries of each lecture, along with copies of handouts and assignments to the course web page and homework solutions.

**TEXT:** John F. Wakerly *Digital Design: Principles & Practices*
Third Edition, Updated., Prentice-Hall, 2001.

Author's website:
`http://www.ddpp.com/student/student.html`
Solutions to selected problems. List of errata for the text

**GRADING:** Homework———20%
Exams————60%
Final Exam——20%

| | |
|---|---|
| A | 90-100% |
| B | 80-89% |
| C | 70-79% |
| D | 60-69% |
| F | $\Downarrow$ 59 |

# Course Policies

## Reading:

You will get more out of each lecture if you complete the reading assignments prior to the lectures. Although you will be responsible for knowing all of the assigned reading material, I will not have time to cover every point presented in the text. Instead, I will focus on the most important points in each section and on questions that you have about the material.

## Homework:

Homework will be assigned and graded. The homework grade will be 20% of your grade for the course. The homework is due at 5:00pm on the day it is due. Homework can be turned in directly to me, to my mailbox, or placed in the COE/EE 243 slot in the cabinet in the second floor hallway of Gauss-Johnson Engineering Lab (located across from room 218). Homework turned in after the due date, but within one week of the due date, will be marked down 25%. Homework over one week late will not be accepted. Solutions will be available on the web page. Homework will be returned in folders that will be located in the hallway of Gauss-Johnson Engineering Lab (across from Room 218). There will probably be 11 assignments. The lowest homework score will be dropped when determining your final grade.

## Midterm Exams:

There will be 5 midterm exams given during the semester. The midterms will count as 60% of your grade. If you have a good reason for missing an exam talk to me **BEFORE** the exam. I will not schedule a makeup exam after the fact.

## Final Exam:

There will be a comprehensive final exam. It will be worth 20% of your final grade. I will drop the lowest score of the 6 exams (midterms and the final).

| Lec # | Date | | Topics | Reading |
|---|---|---|---|---|
| 1 | W | Jan 15 | Intro, Digital Systems, Number Systems | Ch 1, 2.1-2.3 |
| 2 | F | Jan 17 | Binary Addition | 2.4 |
| | M | Jan 20 | Human Rights Day | |
| 3 | W | Jan 22 | Binary Subtraction, Negative Nummbers | 2.4-2.7 |
| 4 | F | Jan 24 | Binary Mult, Divide, Binary Codes | 2.8-2.16 |
| 5 | M | Jan 27 | Logic signals, gates, logic families | 3.1-3.5, 3.10 |
| 6 | W | Jan 29 | Logic families, Combinational Logic | 3.10, 4.1 |
| 7 | F | Jan 31 | Truth tables, basic theorems | 4.1 |
| 8 | M | Feb 3 | Truth tables, minterms, maxterms | 4.1 |
| 9 | W | Feb 5 | Circuit analysis | 4.2-4.3 |
| 10 | F | Feb 7 | Review for Exam #1 | |
| 11 | M | Feb 10 | Exam #1, Chap 1,2,3,4.1-4.3 (partial) | |
| 12 | W | Feb 12 | All NAND, All NOR | 4.3.2 |
| 13 | F | Feb 14 | Minimization, Karnaugh Maps | 4.3 |
| | M | Feb 17 | Presidents Day | |
| 14 | W | Feb 19 | K-maps continued | 4.3 |
| 15 | F | Feb 21 | K-maps continued, Computer methods | 4.4 |
| 16 | M | Feb 24 | Computer Methods, Multiple Outputs | 4.3-4.4 |
| 17 | W | Feb 26 | Review for Exam #2 | |
| 18 | F | Feb 28 | Exam #2, Chapters 4.3-4.4 | |
| 19 | M | Mar 3 | Decoders | 5.4 |
| 20 | W | Mar 5 | Decoders, encoders, multiplexers | 5.5-5.7 |
| 21 | F | Mar 7 | Multiplexers | 5.7 |
| 22 | M | Mar 10 | Comparators, Adders, multipliers | 5.9-5.11 |
| 23 | W | Mar 12 | Documentation, PLDs | 5.1,5.2 |
| 24 | F | Mar 14 | PLDs, Hardware Decription Languages | 5.2,4.6-4.7 |
| | M | Mar 17 | Spring Recess | |
| | W | Mar 19 | Spring Recess | |
| | F | Mar 21 | Spring Recess | |
| 25 | M | Mar 24 | HDL's, Review for Exam #3 | 4.6-4.7 |
| 26 | W | Mar 26 | Exam #3 | |
| 27 | F | Mar 28 | Sequential Logic | 7.1,7.2 |

| Lec # | Date | | Topics | Reading |
|---|---|---|---|---|
| 28 | M | Mar 31 | Latches and Flip-flops | 7.2 |
| 29 | W | Apr 2 | Flip-flops | 7.2 |
| 30 | F | Apr 4 | Flip-flops and State Machines | 7.2, 7.3 |
| 31 | M | Apr 7 | State Machine Analysis | 7.3,7.4 |
| 32 | W | Apr 9 | State Machine Analysis and Timing | 7.4 |
| 33 | F | Apr 11 | Review for Exam #4 | |
| 34 | M | Apr 14 | Exam #4, Chapters 7.1-7.4 | |
| 35 | W | Apr 16 | State machine design, State diagrams | 7.4, 7.5 |
| 36 | F | Apr 18 | State machine design, State diagrams | 7.4, 7.5 |
| 37 | M | Apr 21 | State assignment, state reduction | 7.4, 7.5 |
| 38 | W | Apr 23 | State machines with MSI circuits | 8.2, 8.3 |
| 39 | F | Apr 25 | Sequetial circuits in PLDs, 3-state devices | 8.2,8.3 |
| 40 | M | May 2 | Review for Exam #5 | |
| 41 | W | May 4 | Exam #5, Ch 7 and 8 | |
| 42 | F | Apr 28 | MSI Counters | 8.4 |
| 43 | M | May 5 | MSI Shift Registers, Multipliers | 8.5, 5.10-11, notes |
| 44 | W | May 7 | Memory-ROM, RAM, FPGA, CPLDs | 10.1-10.5 |
| 45 | F | May 9 | Review for final exam | |
| | T | May 13 | Final Exam 10:00 AM – 12:00 Noon | |