Show your work. Do NOT use a calculator!

1. ( 6 pts ) Short answer ( 3 points each)
(a) When designing for a PLA, one is often required to find multiple sum-or-products expressions for each output. Why is this so?
(b) However, when designing for a PAL, one is only required to find the minimal sum-of-products expressions for each output. Why is this so?
2. (6 pts) Realize the three output function shown below using a 3-to-8 decoder and the appropriate logic gates.

$$
\begin{aligned}
& f_{1}(a, b, c)=a b+b^{\prime} c \\
& f_{2}(a, b, c)=\left(a+b^{\prime}+c\right)\left(a^{\prime}+b\right)
\end{aligned}
$$

3. (6 pts) Use a PLA to realize a 4-to-1 multiplexer.
4. (6 pts) Implement $f(A, B, C, D)=A C^{\prime} D^{\prime}+B^{\prime} D$ using a 4-to-1 multiplexer. Choose the appropriate control inputs.
5. (8 pts) (a) Simplify the following multiple output function for implementation with a PAL, and (b) implement it using the AND-OR based PAL shown below.

$$
\begin{aligned}
& F 1(A, B, C, D)=\sum_{m}(0,2,7,10)+\sum_{d}(12,15) \\
& F 2(A, B, C, D)=\sum_{m}(2,4,5)+\sum_{d}(6,7,8,10)
\end{aligned}
$$



