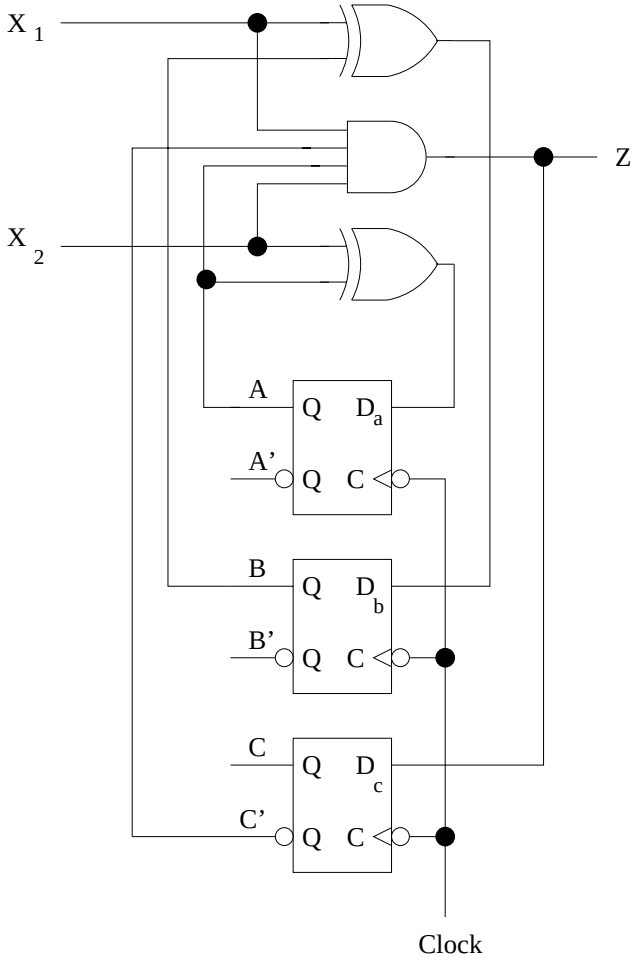
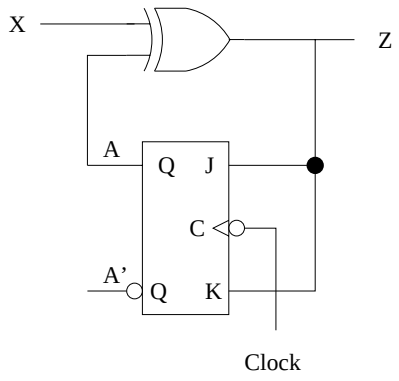
COE/EE 243 **Sample Exam #4** **Original Date: Nov 1998**

NOTE: This was originally a take-home exam, so the problems are a little long

1. (16 pts) Find the transition table and the state table for the Mealy sequential circuit below.



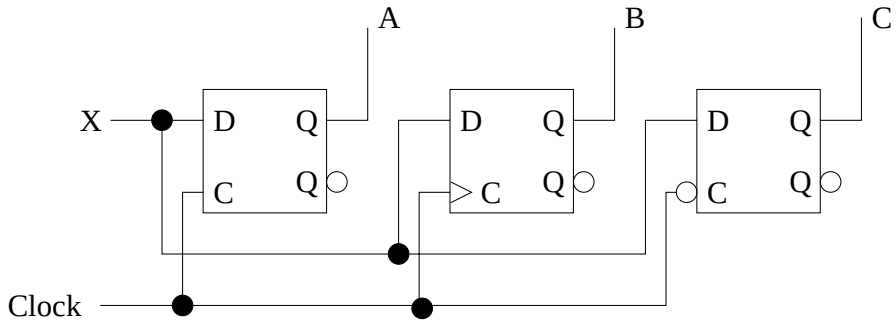
2. (8 pts) The sequential circuit below yields an output sequence of $Z = 11011111$ when you apply the input sequence $X = 01101010$. What is the starting state A?



3. (16 pts) Determine the D flip-flop realization of the sequential circuit specified by the following transition table. Write the combinational logic expressions for the flip-flip inputs and draw the logic circuit diagram.

	A+B+C+		Z	
ABC	X=0	X=1	X=0	X=1
000	001	100	0	0
001	000	010	1	1
010	001	010	0	1
011	010	100	0	0
100	011	000	1	0
101	- - -	- - -	-	-
110	- - -	- - -	-	-
111	- - -	- - -	-	-

4. (10 pts) The circuit below has three D flip-flops, one is level triggered (i.e. triggers based on the level of the clock). The other two are edge triggered, one on the positive-edge and the other on the negative-edge. Complete the timing diagram by filling in the waveforms for *A*, *B*, and *C*.



Propagation delay is assumed to be 1/2 division