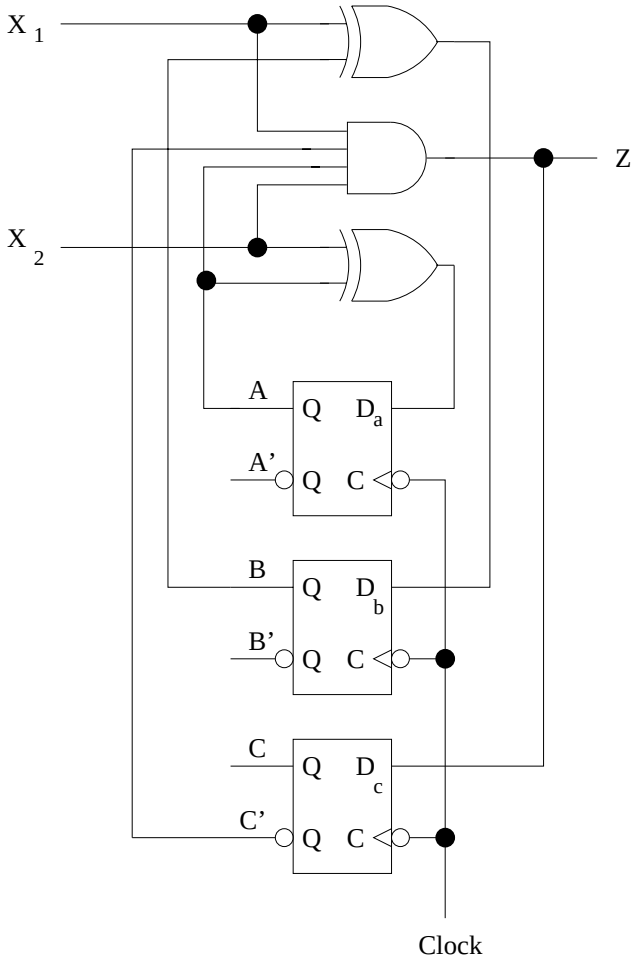
COE/EE 243 **Sample Exam #4 Solution**

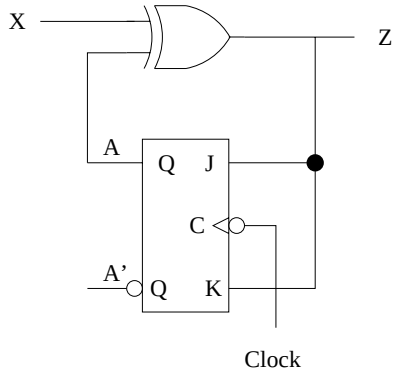
1. (16 pts) Find the transition table and the state table for the Mealy sequential circuit below.



$$\begin{aligned} D_C = Z &= X_1 \cdot X_2 \cdot A \cdot C' \\ D_A &= X_2 \oplus A \\ D_B &= X_1 \oplus B \end{aligned}$$

	$A+B+C+$				Z					$A+B+C+$			
ABC	$X_1X_2=00$	01	11	10	00	01	11	10	ABC	00	01	11	10
000	000	100	110	010	0	0	0	0	S_0	S_0	S_4	S_6	S_2
001	000	100	110	010	0	0	0	0	S_1	S_0	S_4	S_6	S_2
010	010	110	100	000	0	0	0	0	S_2	S_2	S_6	S_4	S_0
011	010	110	100	000	0	0	0	0	S_3	S_2	S_6	S_4	S_0
100	100	000	011	110	0	0	1	0	S_4	S_4	S_0	S_3	S_6
101	100	000	010	110	0	0	0	0	S_5	S_4	S_0	S_2	S_6
110	110	010	001	100	0	0	1	0	S_6	S_6	S_2	S_1	S_4
111	110	010	000	100	0	0	0	0	S_7	S_6	S_2	S_0	S_4

2. (8 pts) The sequential circuit below yields an output sequence of $Z = 11011111$ when you apply the input sequence $X = 01101010$. What is the starting state A?



Since $X = 0$ initially and $Z = 1$, the $A \oplus X = Z = 1$ requires that **A=1** initially.

3. (16 pts) Determine the D flip-flop realization of the sequential circuit specified by the following transition table. Write the combinational logic expressions for the flip-flip inputs and draw the logic circuit diagram.

	A+B+C+		Z	
ABC	X=0	X=1	X=0	X=1
000	001	100	0	0
001	000	010	1	1
010	001	010	0	1
011	010	100	0	0
100	011	000	1	0
101	- - -	- - -	-	-
110	- - -	- - -	-	-
111	- - -	- - -	-	-

Da

CX \ AB	00	01	11	10
00	0	0	X	0
01	1	0	X	0
11	0	1	X	X
10	0	0	X	X

Dc

CX \ AB	00	01	11	10
00	1	1	X	1
01	0	0	X	0
11	0	0	X	X
10	0	0	X	X

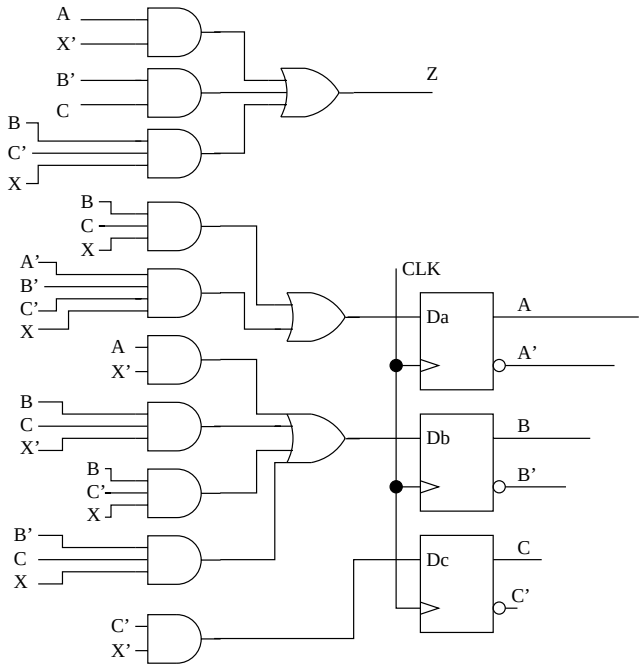
Db

CX \ AB	00	01	11	10
00	0	0	X	1
01	0	1	X	0
11	1	0	X	X
10	0	1	X	X

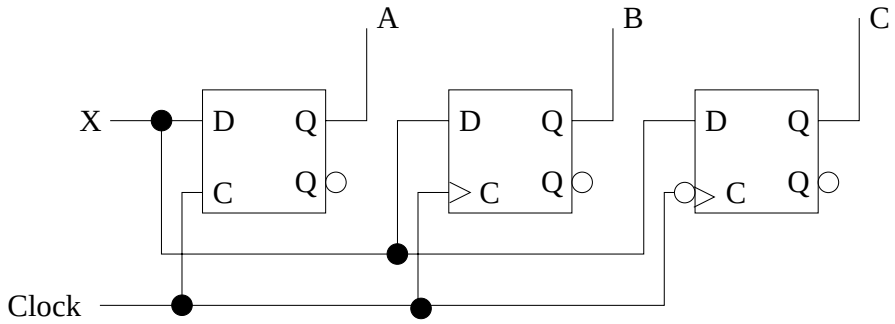
Z

CX \ AB	00	01	11	10
00	0	0	X	1
01	0	1	X	0
11	1	0	X	X
10	1	0	X	X

$A+ = D_A = BCX + A'B'C'X$
$B+ = D_B = AX' + BCX' + BC'X + B'CX$
$C+ = D_C = C'X'$
$Z = AX' + B'C + BC'X$



4. (10 pts) The circuit below has three D flip-flops, one is level triggered (i.e. triggers based on the level of the clock). The other two are edge triggered, one on the positive-edge and the other on the negative-edge. Complete the timing diagram by filling in the waveforms for *A*, *B*, and *C*.



Propagation delay is assumed to be 1/2 division